Nanocrystal embedded MOS non volatile memory devices

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Introduction

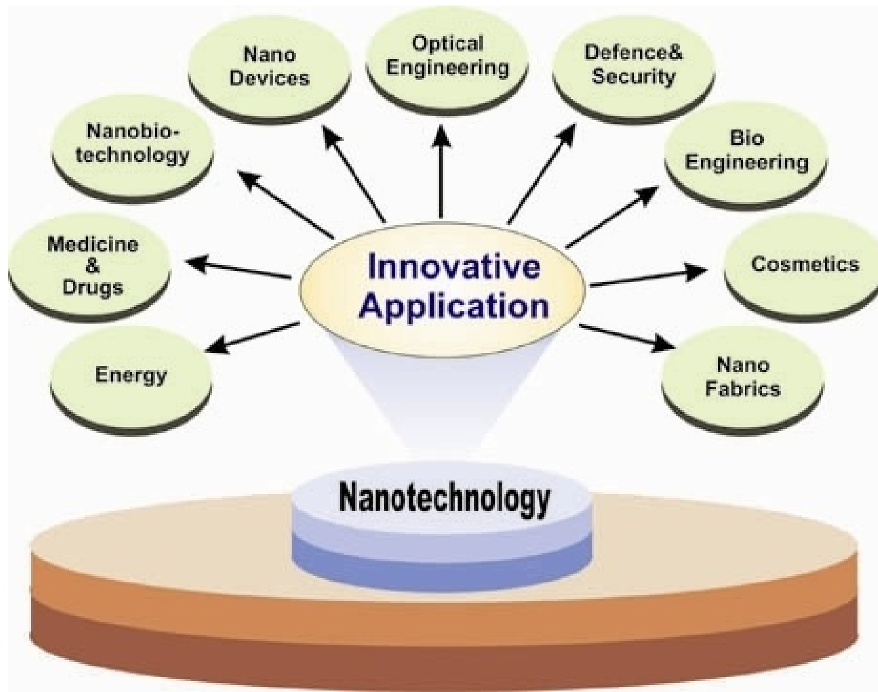
Nanotechnology: A Revolutionary Concept

" There's plenty of room at the bottom"

-Richard P. Feynman

(Caltech, 29.12.1959)

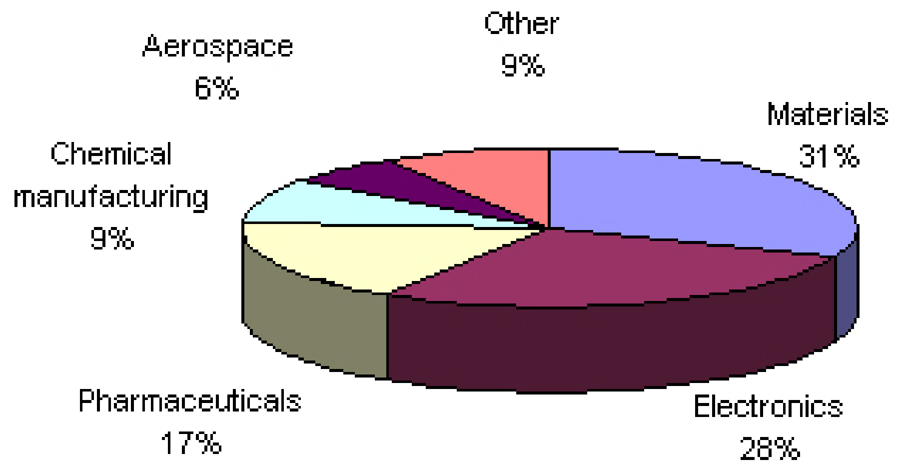
Today Nanotechnology is a vast Inter-disciplinary Field



Source: http://lib.bioinfo.pl/blid:1739

The applications of Nanotechnology are numerous

Nano-electronics holds a major share in this



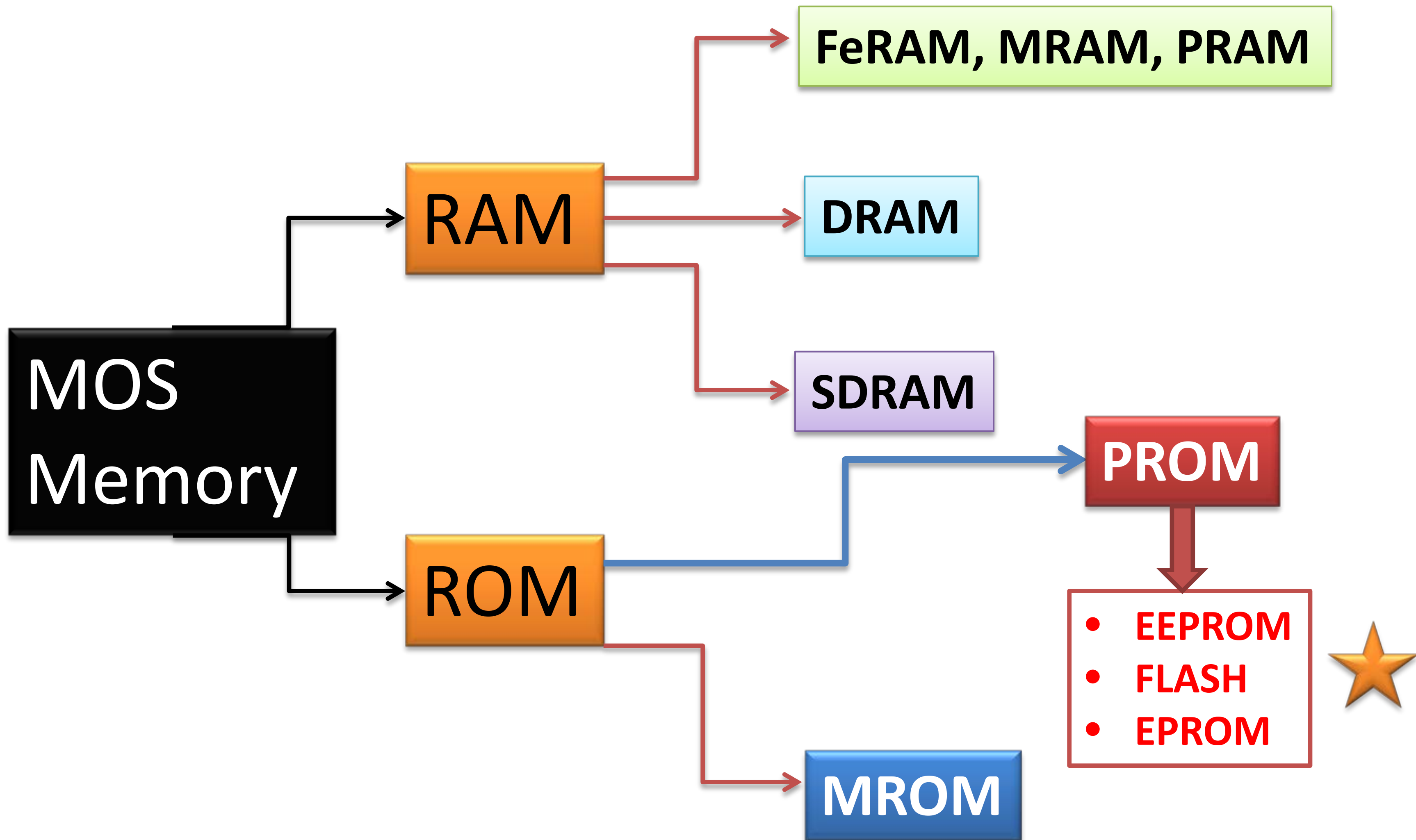
Source: NATIONAL SCIENCE FOUNDATION, USA

MOS Memory Devices

✓USB Flash drives
✓Memory cards (SD,MMC,M2) used in mobile phones, digital cameras, MP3 players
✓Computer DRAMs, Solid State Hard Drives (HDD)
& many more

They are everywhere

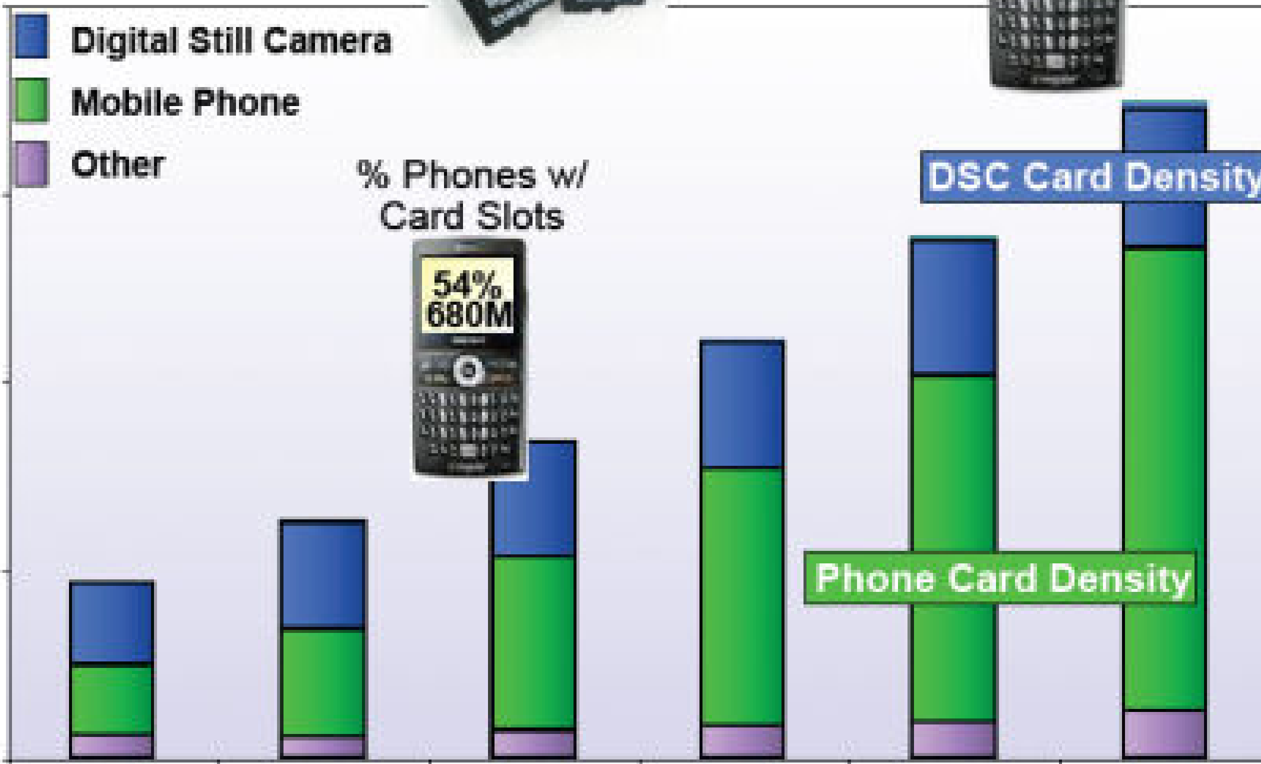
Various MOS Memory Devices



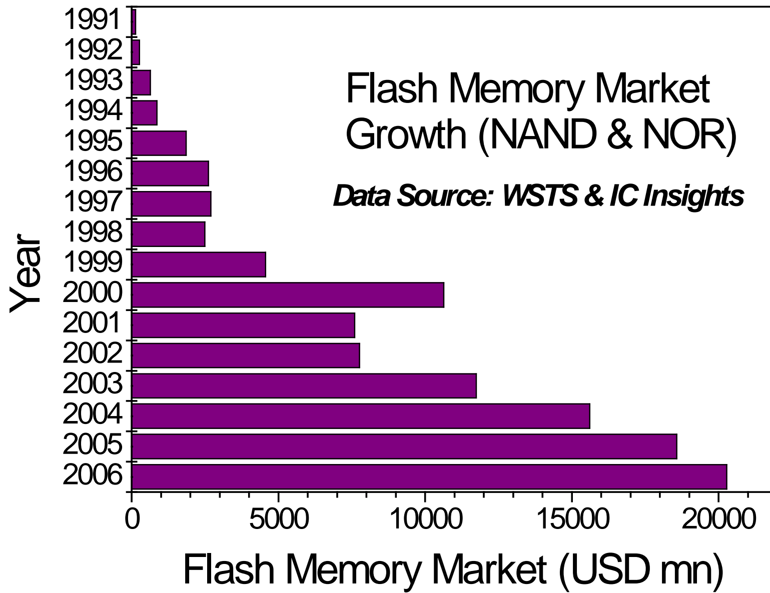
Ref: A. Sengupta, C.K. Sarkar, The 4th IEEE International NanoElectronics Conf. (IEEE INEC), June 21-24, 2011, Taiwan

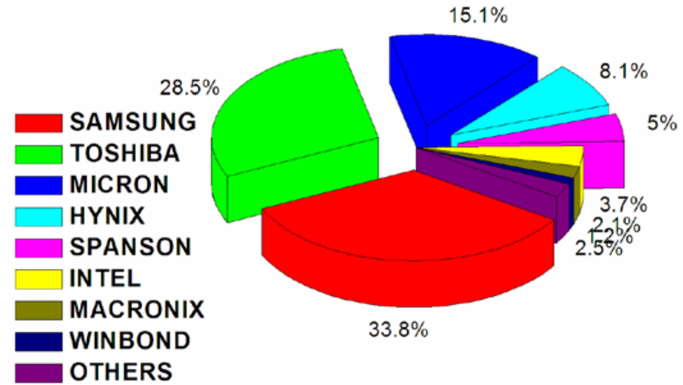
Flash Card Market Growth

Avg
Card
GB



*Source : SEC Marketing





Inside the chip factory

The Oregonian

CLICK HERE to see the chip-making process in action, then rollover the red squares to learn more about the factory.

Intel has invented a faster, more efficient computer chip, along with a process for manufacturing it. This illustration depicts, in condensed form, the operation of a $3 billion factory. An actual factory, is nearly 1 million square feet — big enough to house three Boeing 747s.

FAB LEVEL

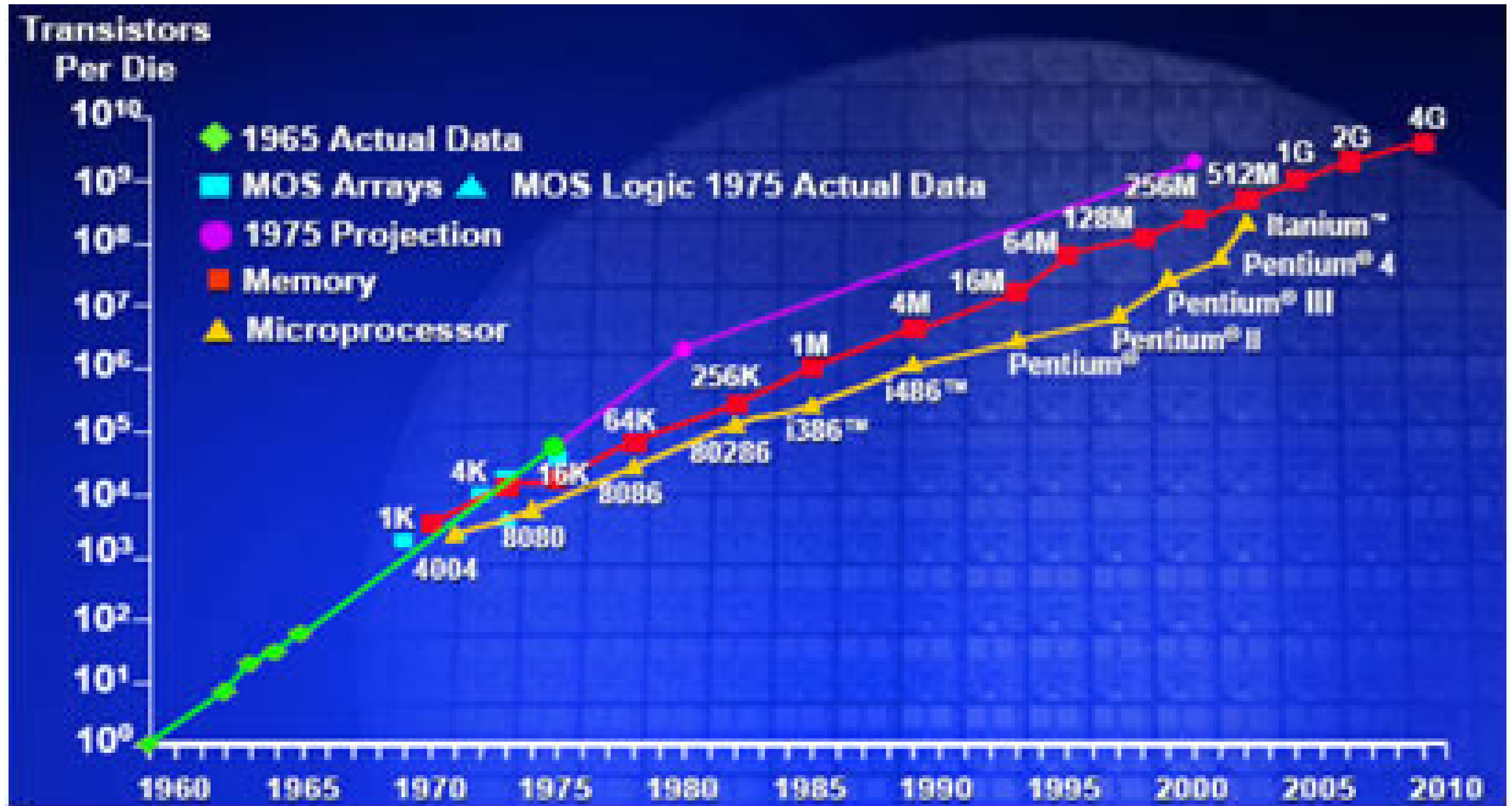
SUB-FAB LEVEL

Intel's production tools cost $1 million apiece or more, and there are hundreds in every factory - $2 billion worth, all told. Each must be finely calibrated to match the performance of the tools in Oregon that Intel used in developing its chip. The machines usually function automatically, with technicians monitoring to ensure they meet exacting specifications.

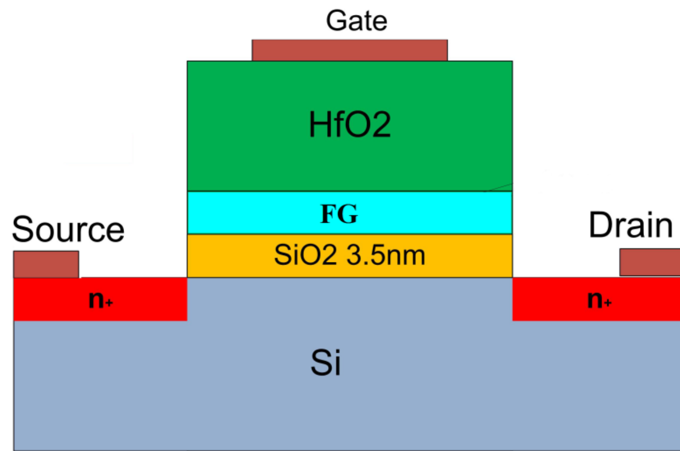
The sub-fab, a full story tall beneath the factory floor, provides power, chemicals, water and gases. Pumps and chillers support the tools.

Illustration by STEVE COWDEN

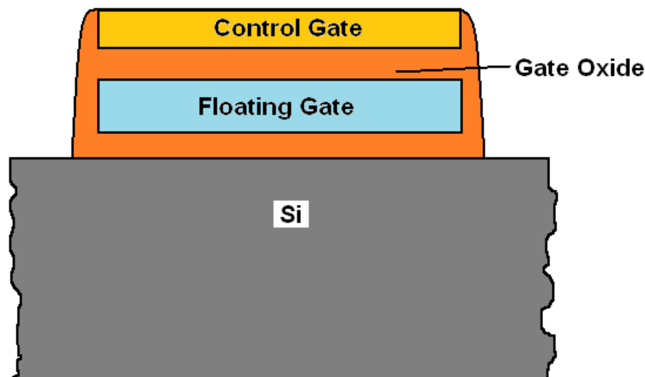
Transistors per die of MOS Memory Devices

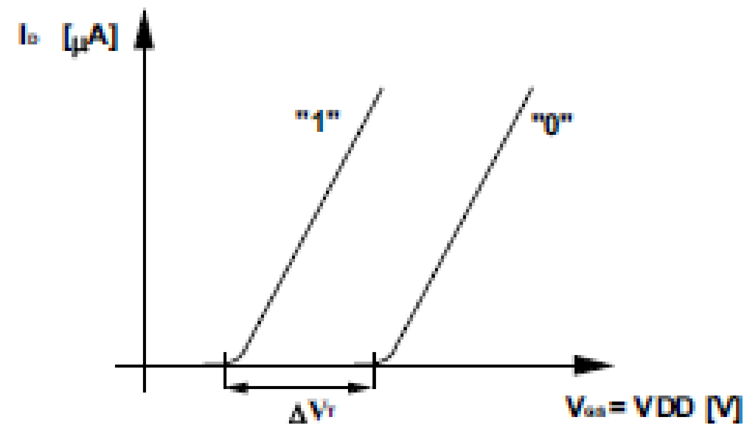


MOSFET memory and MOS capacitors



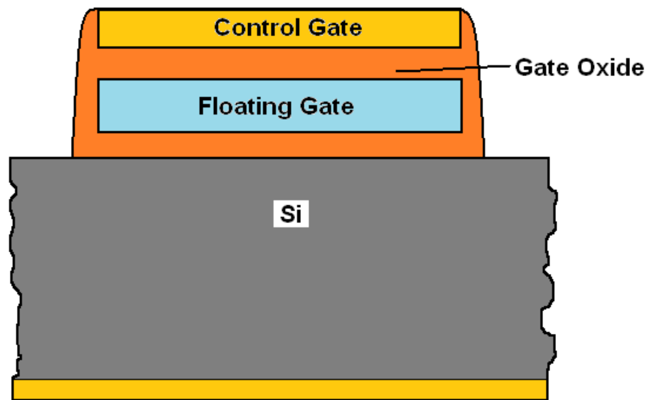
MOSFET memory devices rely on charge stored in the Floating Gate to cause a shift in the threshold/ flatband voltage.





Campardo et. al. VLSI Design of Non-Volatile Memories, Springer Verlag, Berlin Heidelberg 2005, pp. 50

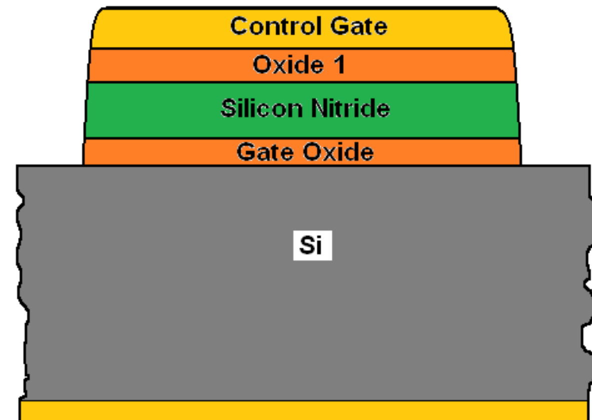
Conventional MOS NVMs : Floating gate & SONOS



Floating Gate MOS memory device

✓Charges are stored in the polysilicon Floating Gate.
✓Most commonly used for Flash memory applications.

✓Charges are stored in the Oxide-Nitride interface.
✓Another variant MNOS useful for Aerospace/Military applications.



SONOS MOS memory device

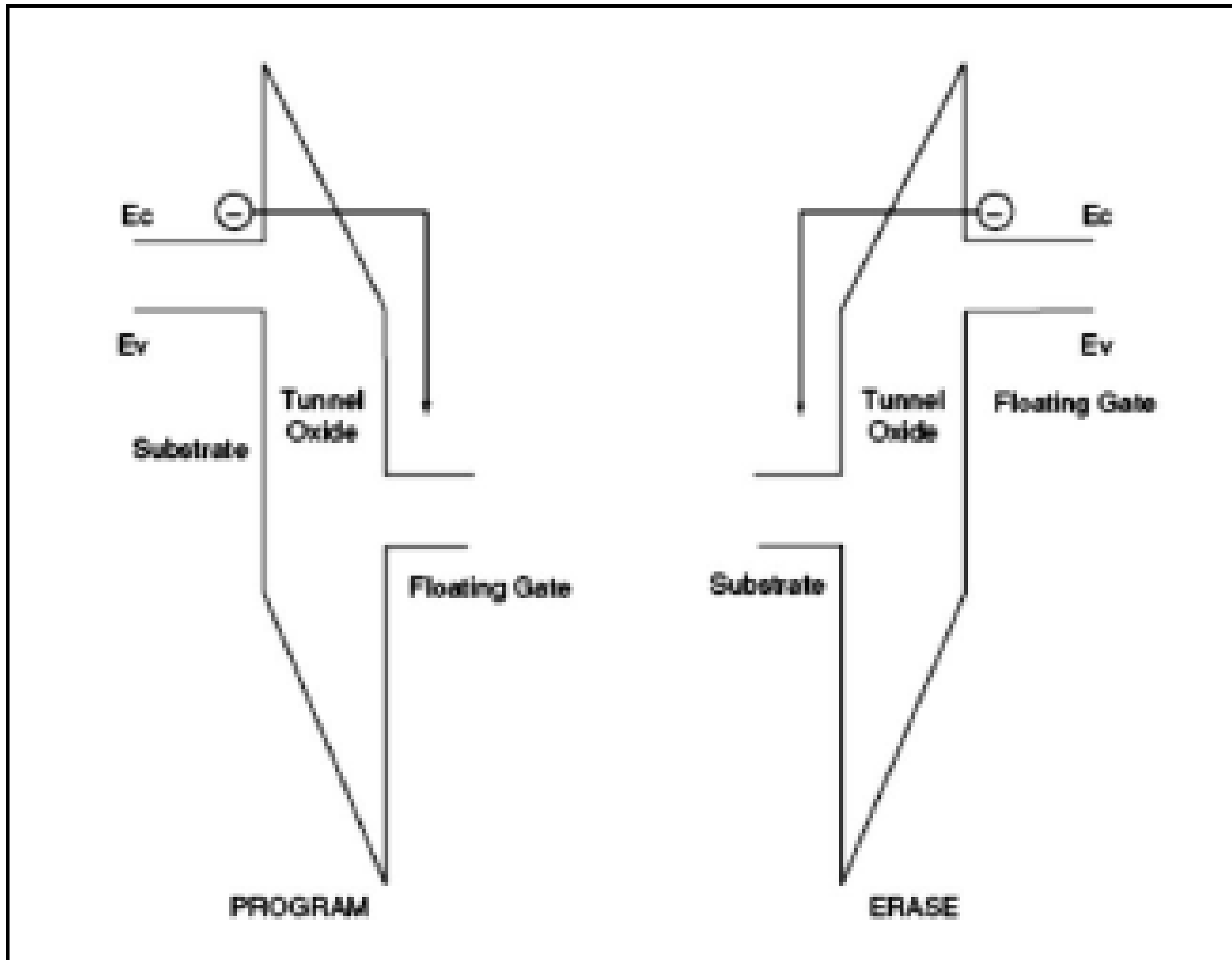
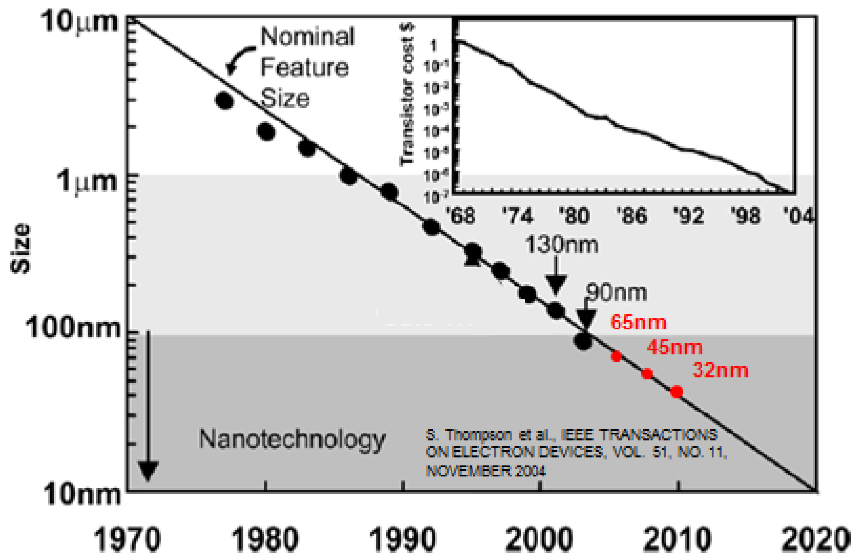


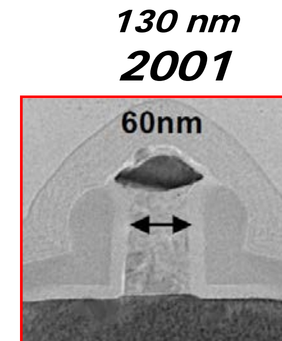
Fig. 2.3: Band diagrams of a Program /Erase operations of a floating gate cell

(Ref: Micheloni et. al. Inside NAND Flash memories, Springer pp.91)

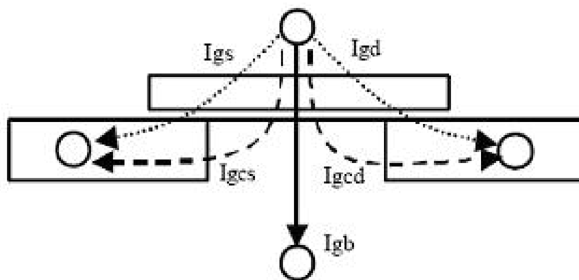
Disadvantage of conventional MOS Memory Devices

- **With scaling and thinner tunnel oxides, leakage provides a major challenge.**
- **Also for portability lesser write voltages are required.**
- **Advantages of Nanotechnology may be applied to MOS devices.**
- **Nanocrystal embedded MOS NVMs can help in this regard.**

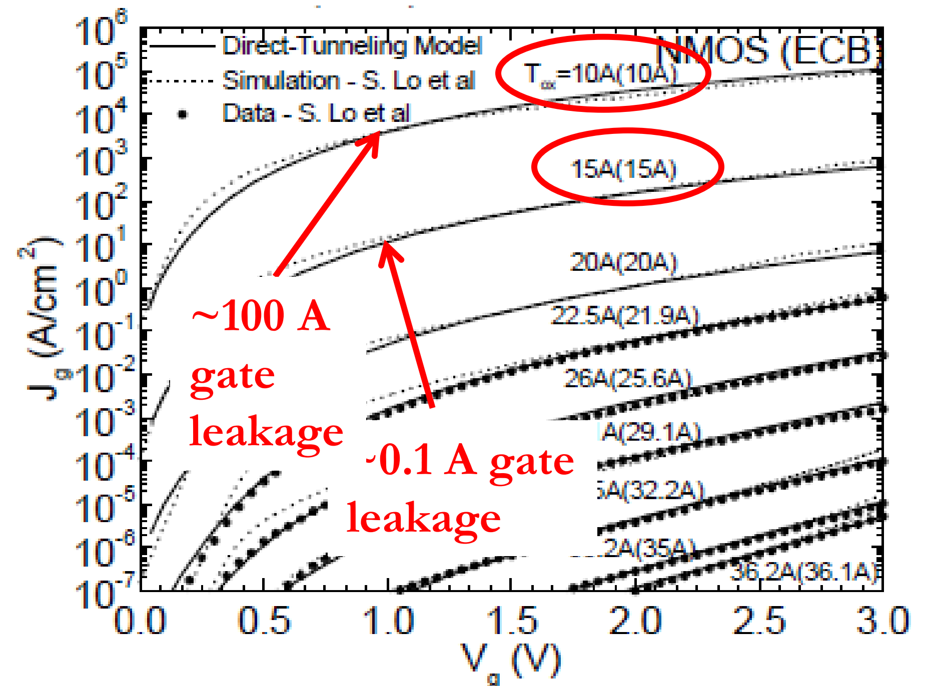




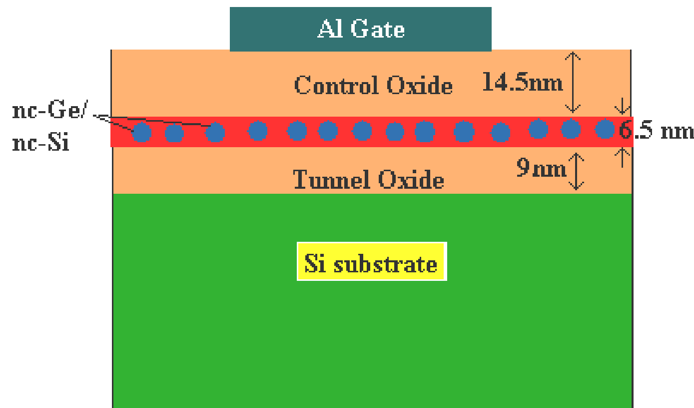
Courtesy : Prof. Jakub Kedzierski
IIT-Bombay/ MIT Lincoln Lab

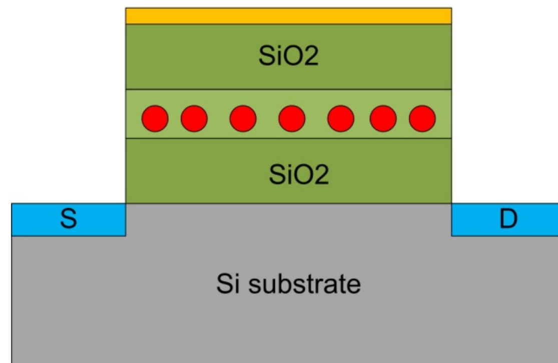


Road-block: *Gate oxide tunneling current, the quantum nature of matter lets electrons penetrate the gate oxide*



Nanoparticles Based Floating Gate MOS Memory Structure

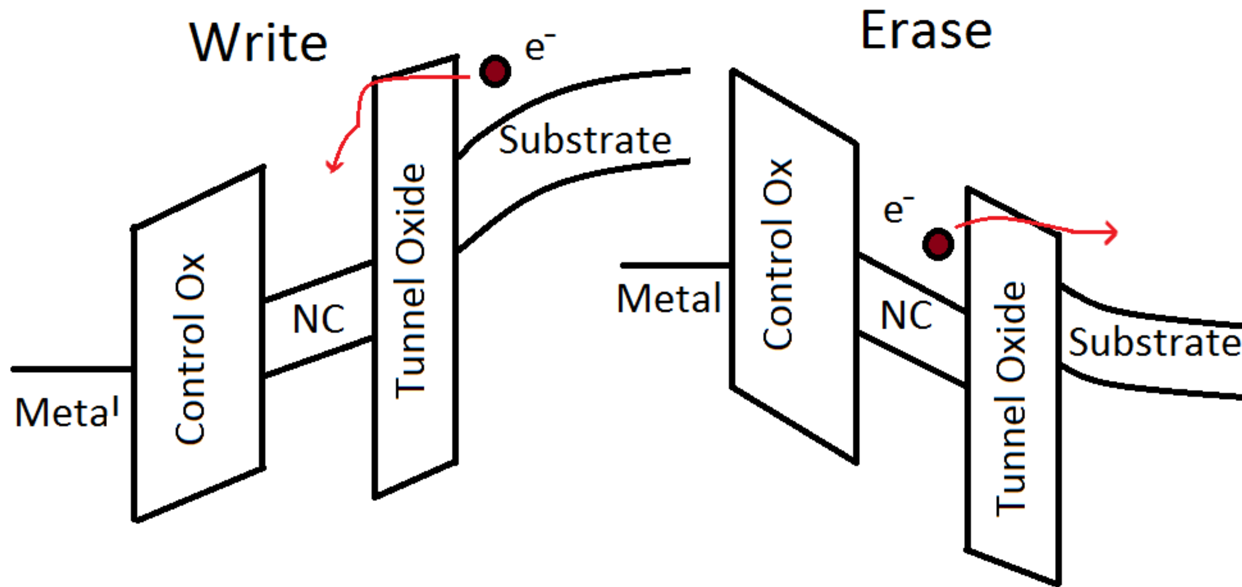


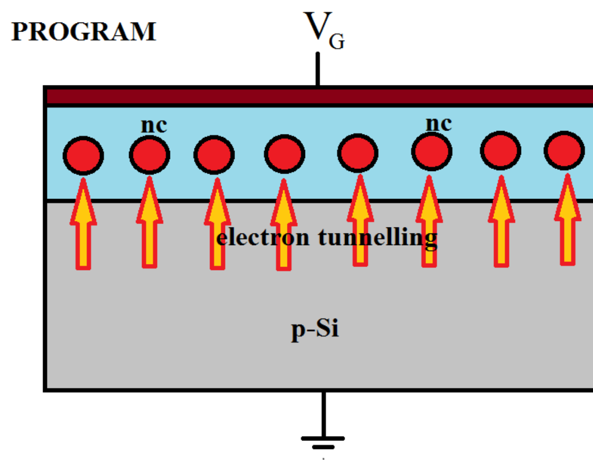


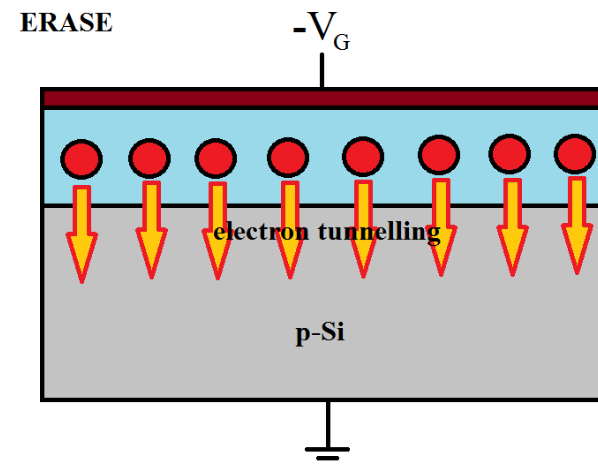
Nanoparticles embedded floating gate MOSFET and MOSCAP

- Nanoparticles(nc) diameter in 5-6nm range.
- Confined in a narrow layer within SiO_2 called embedded gate dielectric
- Charging and discharging of nc carried out by electron tunneling
- Electrons tunnel from Si substrate to gate electrode through gate dielectric
- A thin tunneling barrier is formed at the interface of silicon substrate and composite gate dielectric
- Comparison of nc-Si and nc-Ge embedded gate oxide MOS devices.

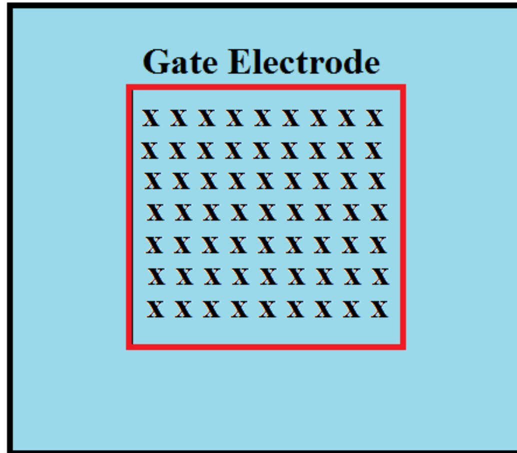
Write/Erase mechanism of such a device

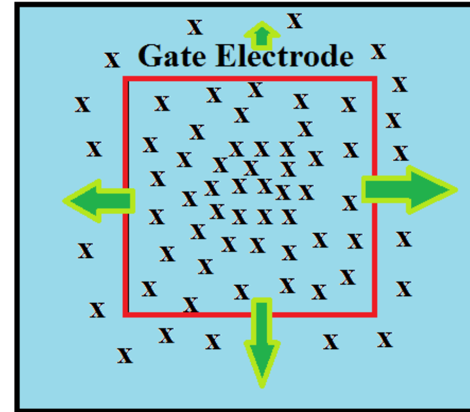


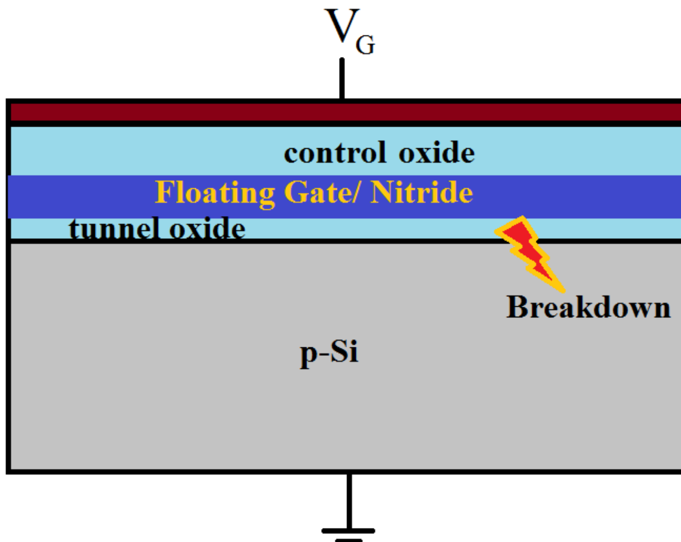


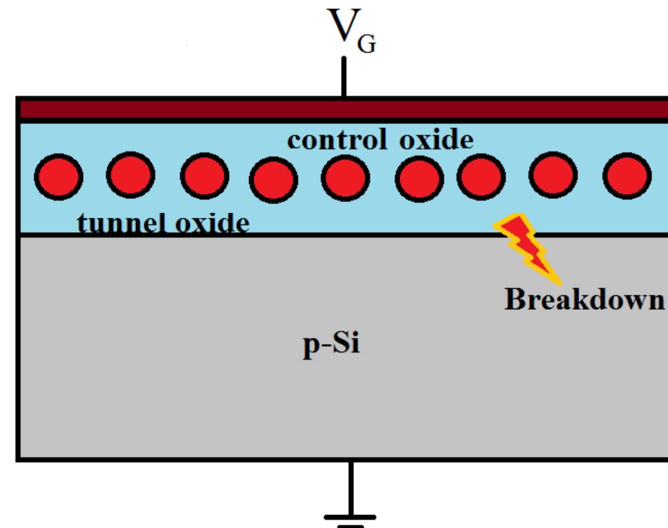


Advantages of Nanocrystal embedded MOS NVM





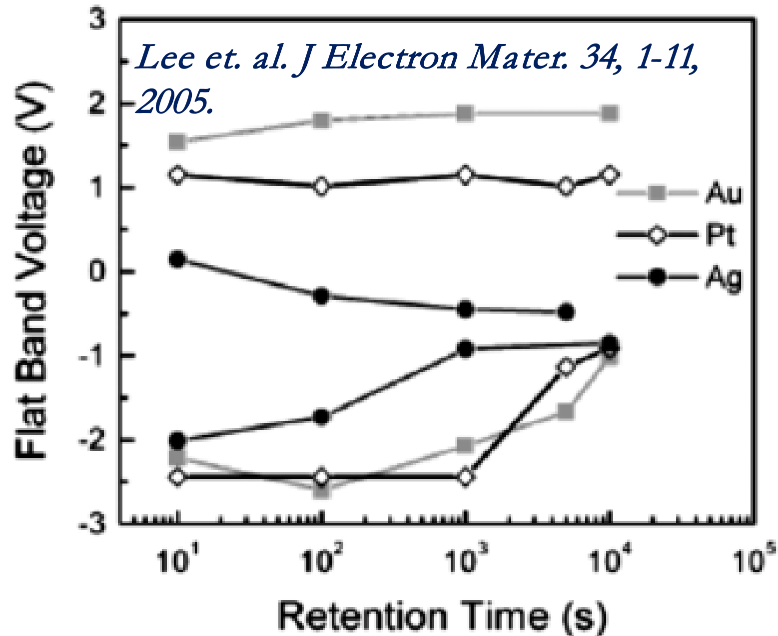


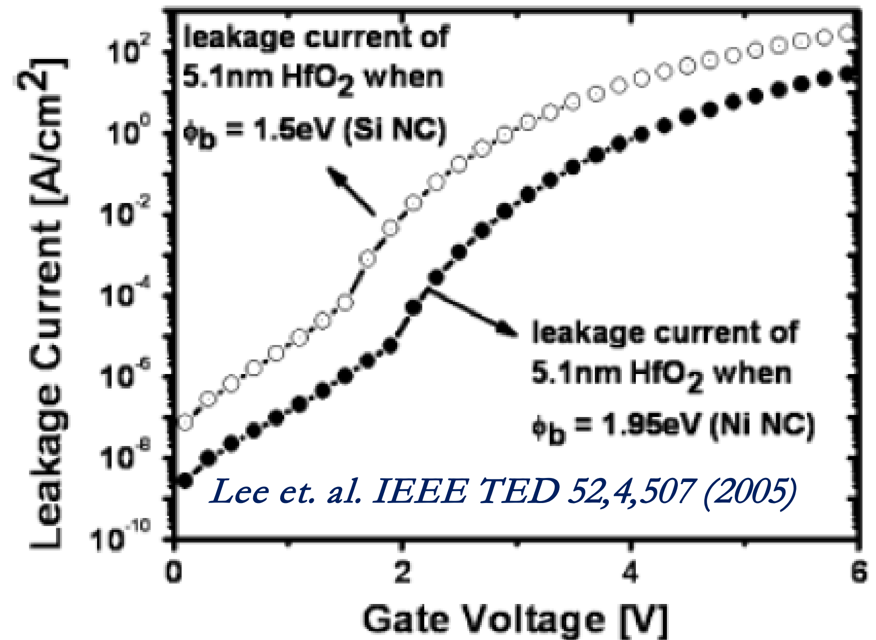


Recent Developments

Metallic Nanocrystals

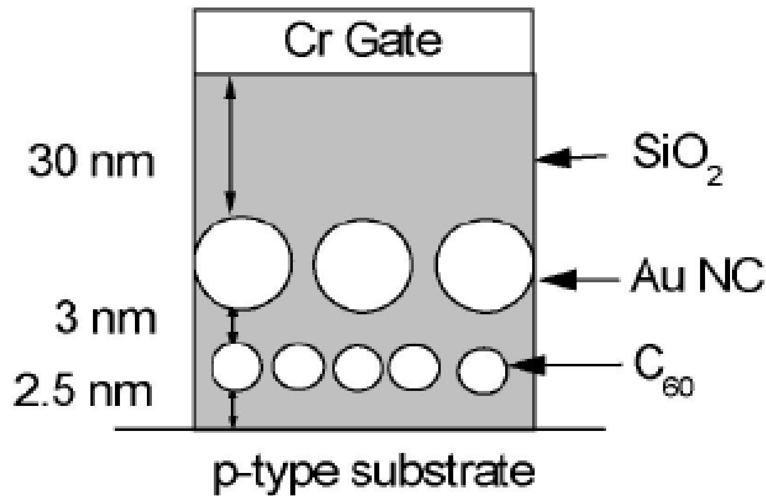
Use of Metallic nanocrystals like Ni, W, Ag, Au, Pt ncs.

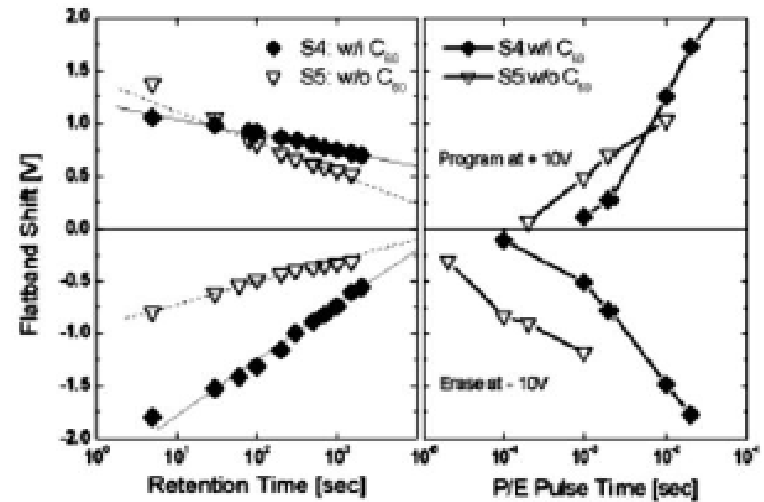




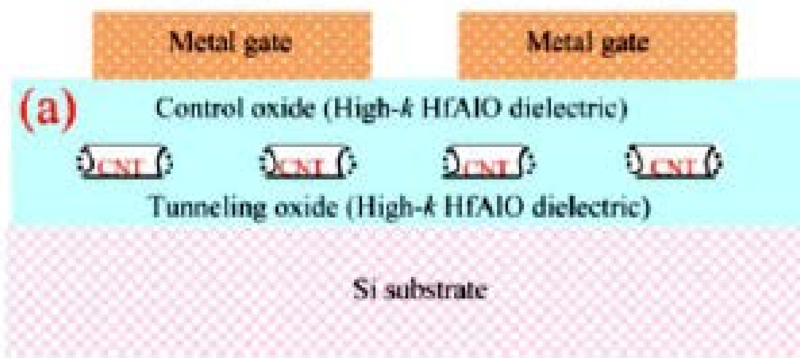
Better charge storage , Lesser leakage, improved retention

CNT/ C60 embedded MOS NVM

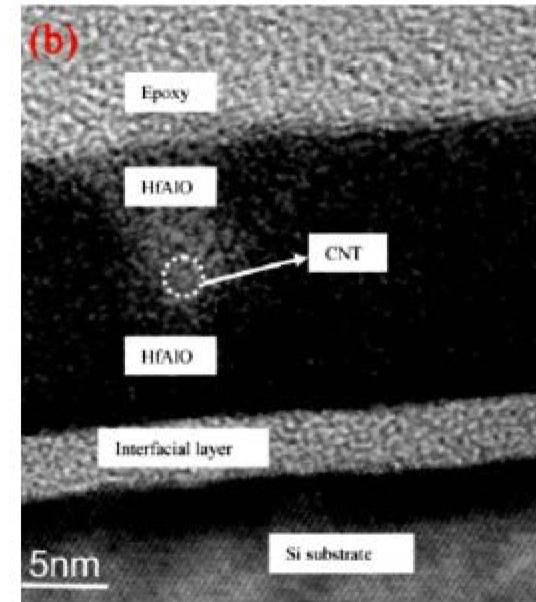




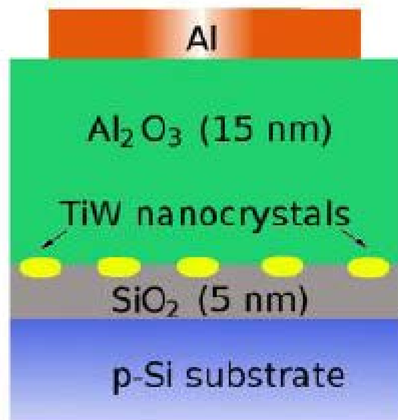
[T-H. Hou et. al. Device Research Conference, 2008, Issue Date: 23-25 June 2008 pp.275 - 276



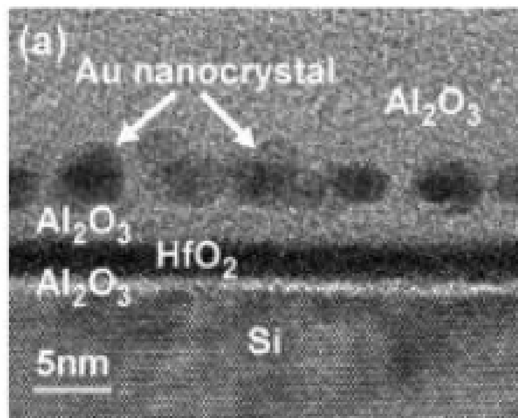
[X. B. Lu and J. Y. Dai, Applied Physics Letters, vol. 88, no. 11, p. 113104, 2006.]



Stacked High-k gate dielectrics



Yang et. al. Nanotechnology 21 (2010) 245201

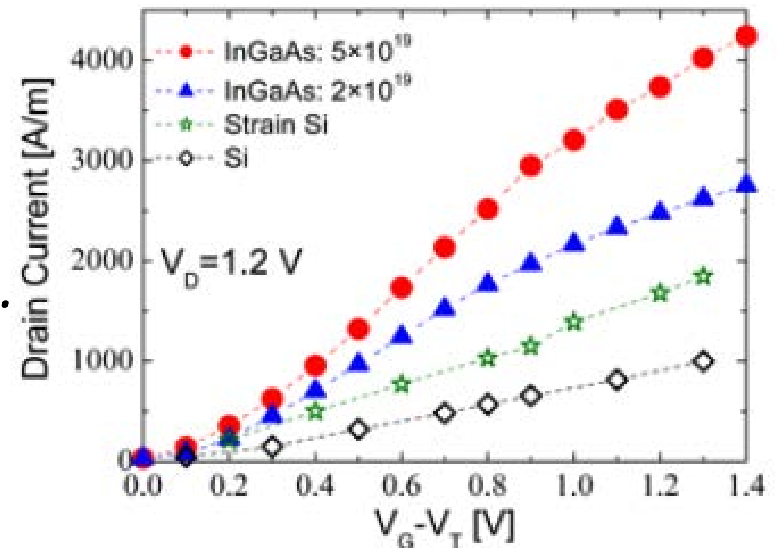


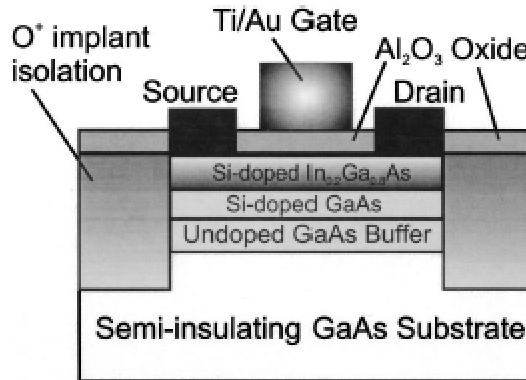
Lo et. al. APPLIED PHYSICS LETTERS 94, 082901 2009]

- *High-k materials help in suppressing the leakage.*
- *They have better charge retention then SiO_2 gate dielectrics.*
- *Better Program / Erase cycles endurance.*

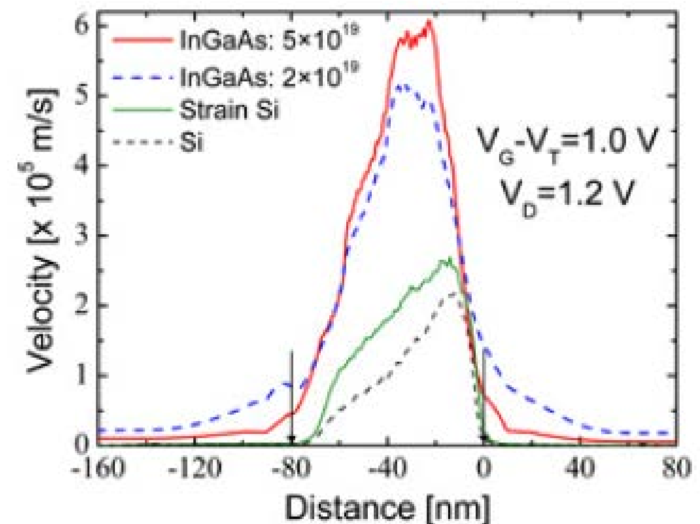
Compound semiconductor MOSFET

- *Compound semiconductors like $In_xGa_{1-x}As$, GaN, InP, GaAs have better MOSFET performance than conventional Si or strained Si MOS.*
- *Such compound semiconductor MOS can be used for memory applications as well.*



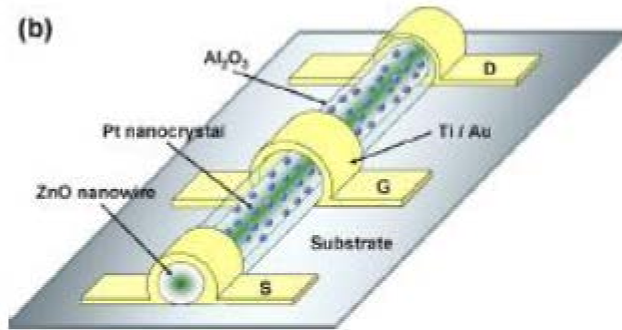


P. D. Ye et alApplied Physics Letters, vol. 84, no. 3, p. 434, 2004.

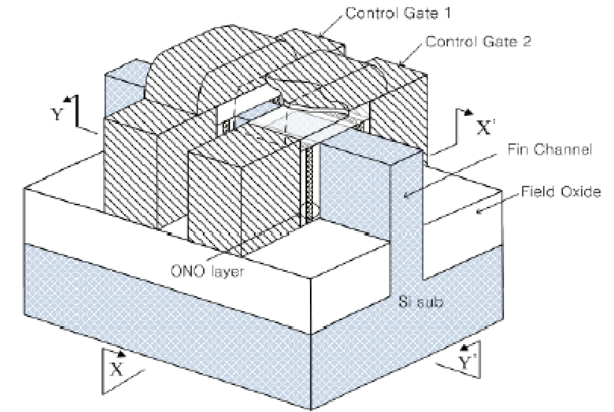


Kalna et. al. Semicond. Sci. Technol. 19 S202-S205 (2004)

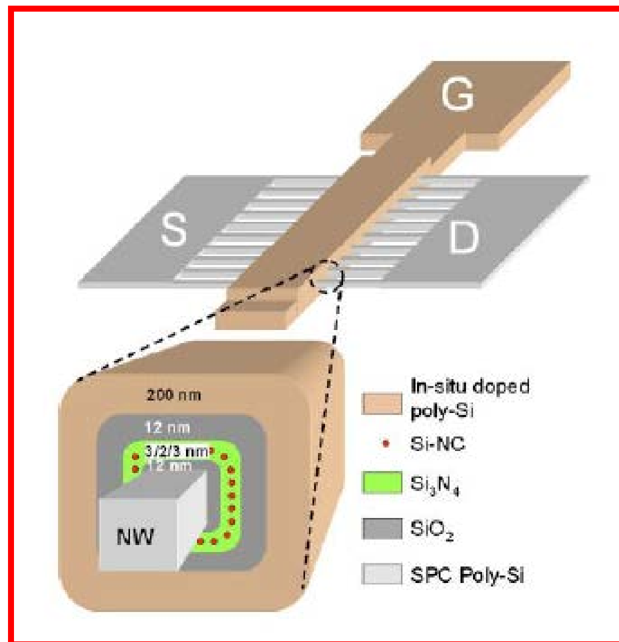
Multigate MOS NVM structures



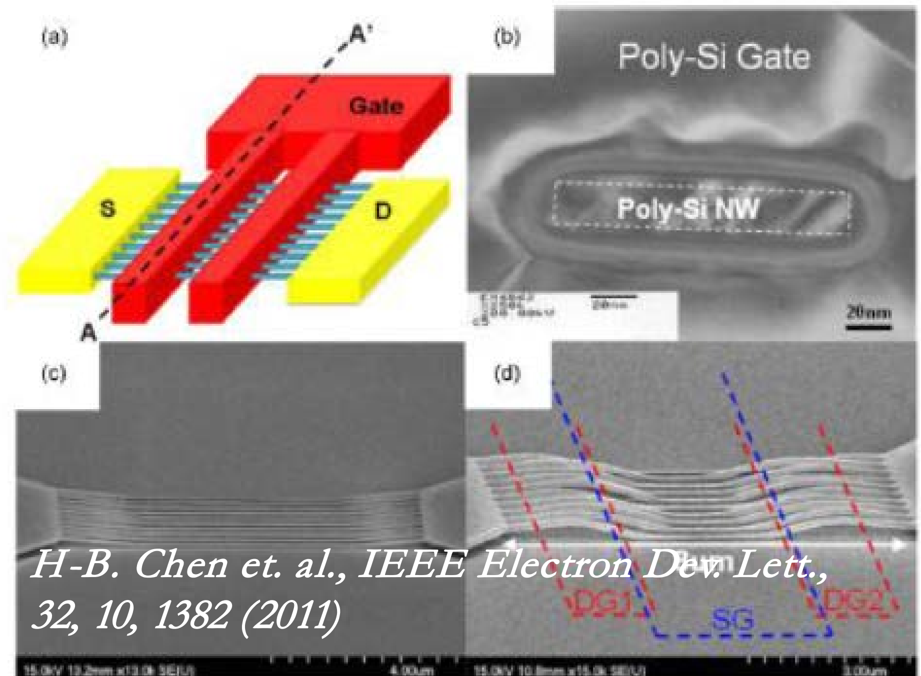
Yeom et. al. Nanotechnology 19 (2008) 395204



S. Oh, J. Kor. Phys. Soc., 55, 1, 263, 2009



M.F. Hung, Applied Physics Letters, 98, 162108, 2011



H-B. Chen et. al., IEEE Electron Dev. Lett., 32, 10, 1382 (2011)

Modeling of MOS Non-Volatile Memories

Why Modeling?

- ***Many device structures, many materials in terms of the embedded NCs and the substrate materials.***

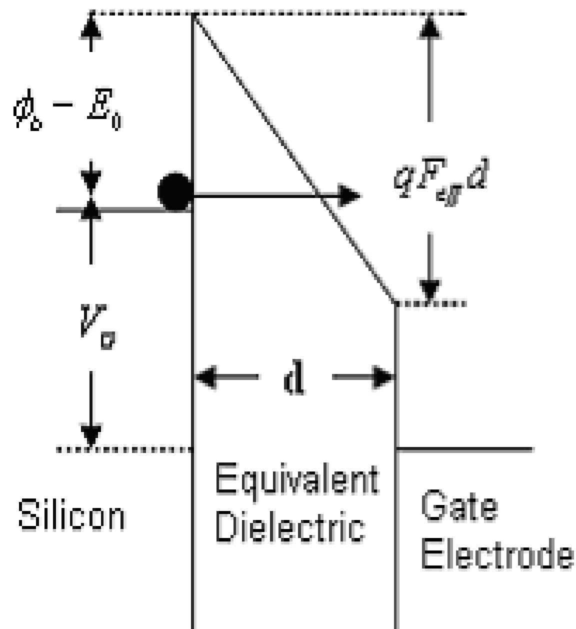
- ***Fabrication and testing is costly, time-consuming and requires infrastructure and manpower.***

- ***A good model can thus act as a pointer in the right direction well before the actual fab is carried out.***

Need for New Simulations

- *Standard device simulators like Sentaurus, Silvaco TCAD do not incorporate nanocrystal embedded MOS NVMs.*
- *Existing models are either involving a large amount of numerical solutions and rather complex iterative orthogonalization and extraction methods for 3D Kohn-Sham / Poisson-Schrodinger equations.*
- *No analytical models for advanced multi-gate nc embedded gate dielectric MOSFET NVMs.*

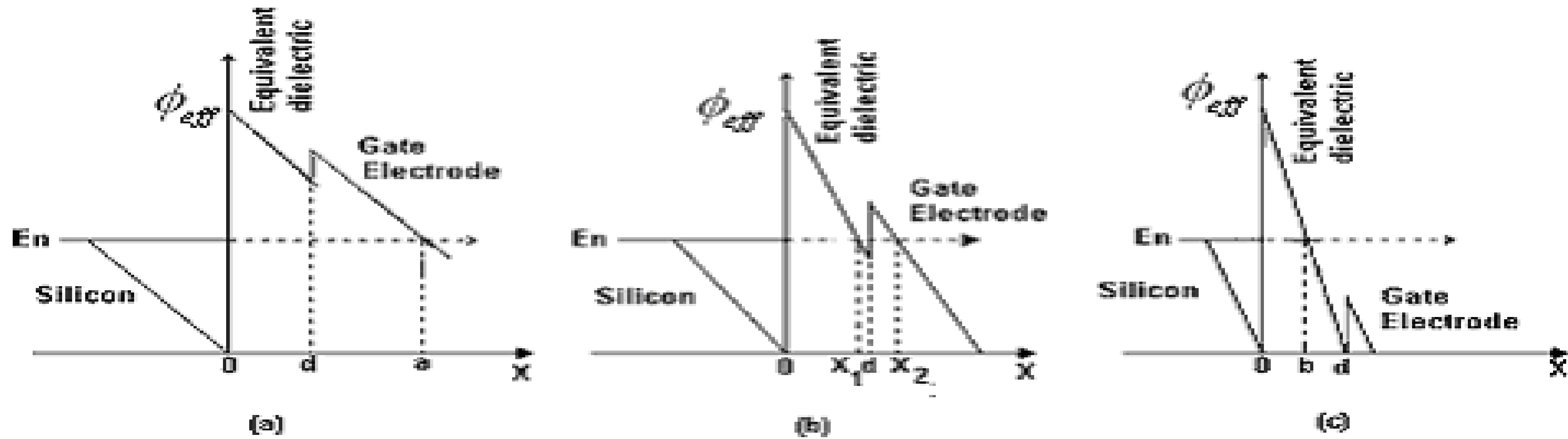
Write Mechanism: Fowler – Nordheim Tunneling



- High Applied Gate voltage → Fowler-Nordheim tunneling
- The barrier becomes Triangular in shape
- Applied gate voltage $V > (\phi_{eff} - E_0)/q$
- Electrons tunnel from the conduction band of Si to conduction band of oxide through part of potential barrier

Band diagram of Fowler-Nordheim tunneling

Band Structure of Tunneling under Different Conditions of Applied Electric Field



Band bending at applied electric fields under different conditions (a) $F_{eff}d < \phi_{eff} - E_n$

(b) $\phi_{eff} - E_n < F_{eff}d < \phi - E_n$ (c) $F_{eff}d > \phi - E_n$

F-N Tunneling Probabilty

Case I : $qF_{eff}d < \left(\phi_{eff} - E_o\right)$

$$D\left(E_0\right) = \exp\left(-\frac{4\sqrt{2m_{eff}}}{3q\hbar F_{eff}}\left[\left(\phi_{eff} - E_0\right)^{3/2} - \left(\phi_{eff} - E_0 - qF_{eff}d\right)^{3/2}\right] - \frac{4\sqrt{2m}}{3q\hbar F}\left(\phi - E_0 - qF_{eff}d\right)^{3/2}\right)$$

Case II : $\left(\phi_{eff} - E_o\right) < qF_{eff}d < \left(\phi - E_o\right)$

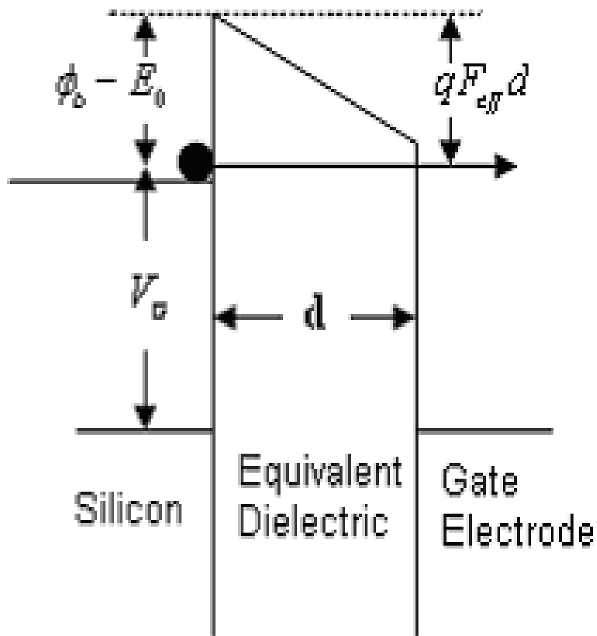
$$D\left(E_0\right) = \left\{\sin^2\theta_2\cosh^2(\theta_3 - \theta_1) + \cos^2\theta_2\cosh^2\left[\theta_3 + \theta_1 + \ln(4)\right]\right\}^{-1}$$

$$\hbar\theta_i = \int_{x_{i-1}}^{x_i}\left\{2m^*\left\|\left[V\left(x\right) - E_0\right]\right\|\right\}^{1/2} dx$$

Case III : $qF_{eff}d > \left(\phi - E_o\right)$

$$D(E_0) = \exp\left(-\frac{4\sqrt{2m_{eff}}}{3q\hbar F_{eff}}\left(\phi_{eff} - E_0\right)^{3/2}\right)$$

Leakage: Direct Tunneling



- Low Applied Gate voltage → Direct tunneling
- Applied gate voltage condition
- The Barrier becomes Trapezoidal in s $V < (\phi_{eff} - E_0)/q$
- Electrons tunnel directly from Si conduction band to metal instead of through oxide conduction band

Band diagram for direct tunneling

$$J_D = \frac{\{2m_{eff}(\phi_{eff} - E_0)\}^{1/2} \alpha q^2 V}{\hbar^2 d} \exp\left(\frac{2\alpha\sqrt{2m_{eff}(\phi_{eff} - E_0)}}{\hbar} d \right)$$

Parameters changed due to inclusion of Nanoparticles

- Dielectric constant of SiO_2 embedded with nc-Si determined by using Maxwell-Garnett Effective Medium Approximation (EMA)

$$\in_{nc-ox} = \frac{\in_{ox}\left\{2\nu\left(\in_{nc} - \in_{ox}\right) + \left(\in_{nc} + 2\in_{ox}\right)\right\}}{\in_{nc} + 2\in_{ox} - \nu\left(\in_{nc} - \in_{ox}\right)} \qquad \in_{eff} = \left\{\frac{t_{ox}}{\in_{ox} \cdot t} + \frac{t - t_{ox}}{\in_{nc-ox} \cdot t}\right\}^{-1}$$

- Band gap energy has been modified

$$E_{gnc} = E_{bulk} + \frac{\hbar^2 \pi^2}{2R^2}\left(\frac{1}{m_h^*} + \frac{1}{m_e^*}\right)$$

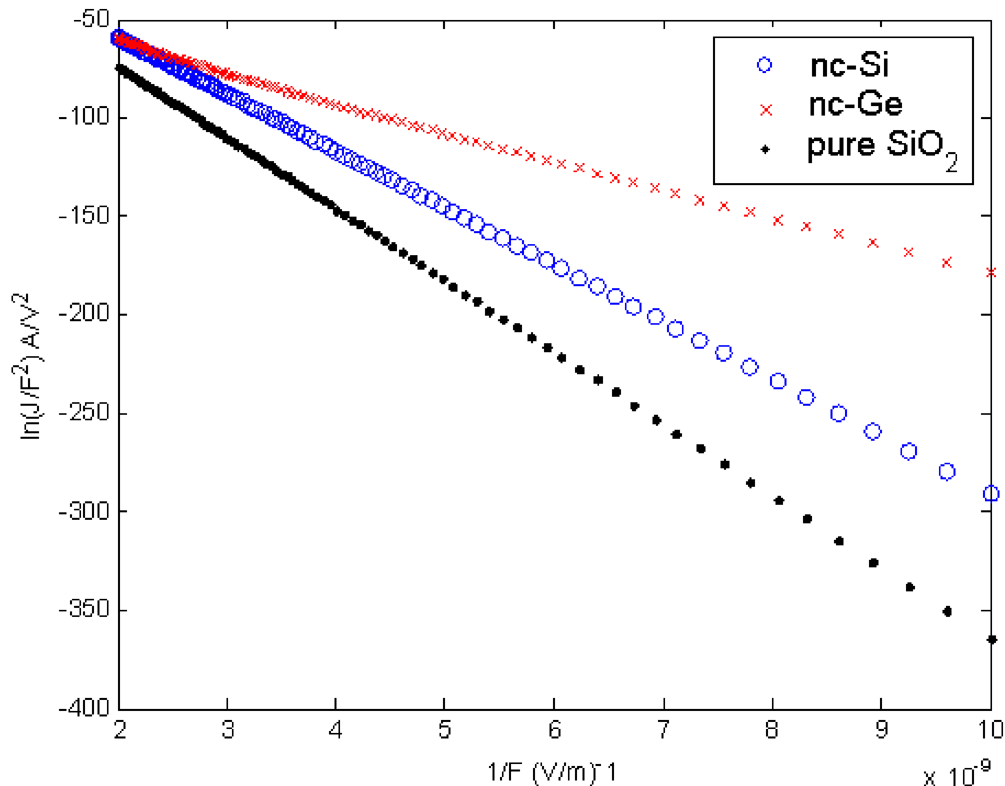
- Effective barrier height modified

$$\phi_{eff} = \frac{1}{2}\left[\frac{E_{gsio2}}{2} + \frac{1}{2}\left(E_{gsio2} \cdot (1-\nu) + \nu \cdot E_{gnc}\right) - E_{gsi}\right]$$

- Electron effective mass has been changed

$$m_{eff} = \left[\frac{m_{sio2} d_{sio2}}{d} + \frac{m_{nc}(d - d_{sio2})}{d}\right]$$

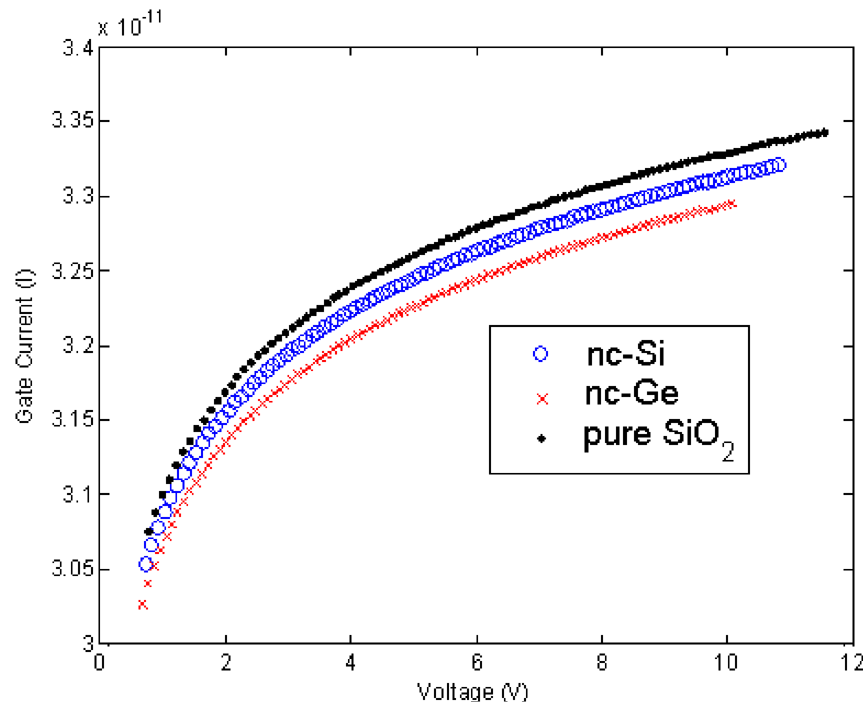
Simulated Fowler-Nordheim Plot



- FN plot compares the pure SiO_2 gate dielectric with the nc-Si and the nc-Ge embedded dielectric.
- Both The nanoparticles embedded composite gate dieletrics show higher F-N tunneling current density than the pure SiO_2 dielectric.
- The F-N tunneling current density is higher in nc-Ge embedded gate dielectric than the nc-Si embedded one.

Ref: G. Chakraborty, A. Sengupta, F.G. Requejo, C.K. Sarkar, J. Appl. Phys., 109, 064504 (2011).

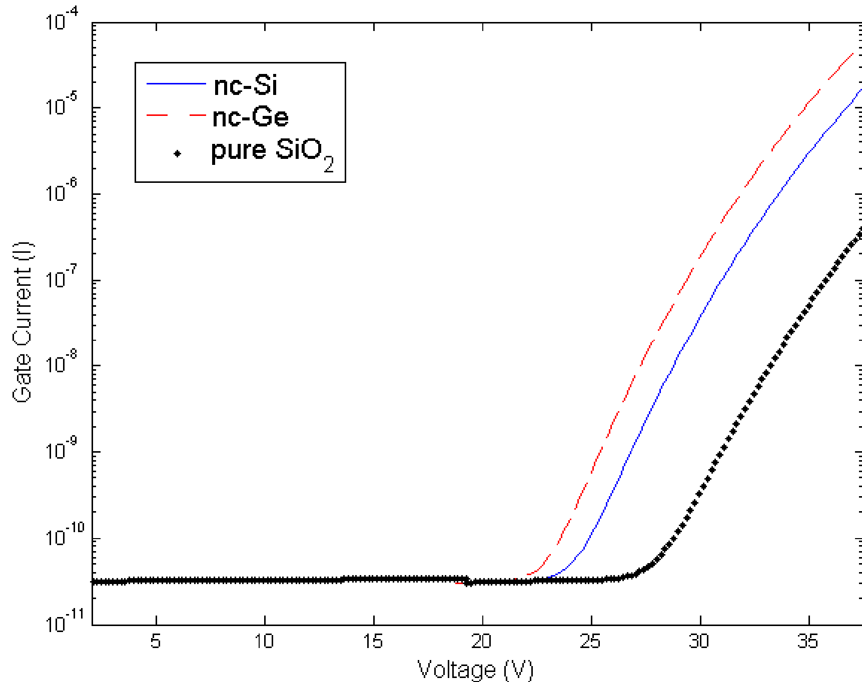
Simulated Leakage Current



- Here it is seen that the incorporation of nanocrystals in the gate oxide somewhat reduces the direct tunneling (leakage) current compared to pure SiO_2 gate. Also it is evident that for the nc-Ge the value of the direct Tunneling current is the least.

Ref: G. Chakraborty, A. Sengupta, F.G. Requejo, C.K. Sarkar, J. Appl. Phys., 109, 064504 (2011).

Simulated I-V Characteristics



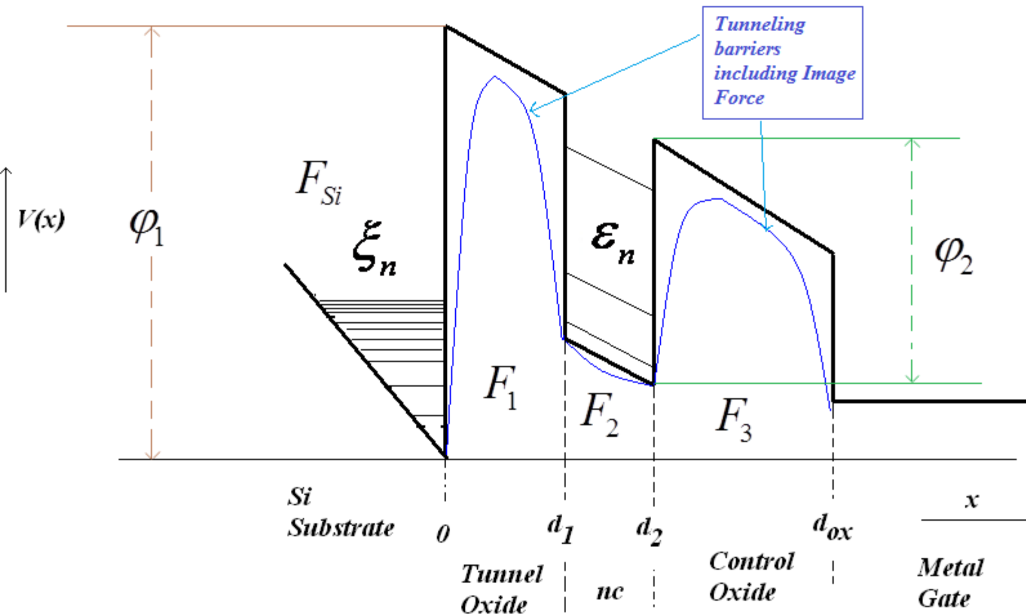
▪Nanocrystalline particles embedded gate oxide has an F-N tunneling current few decades greater compared to pure SiO_2 gate.

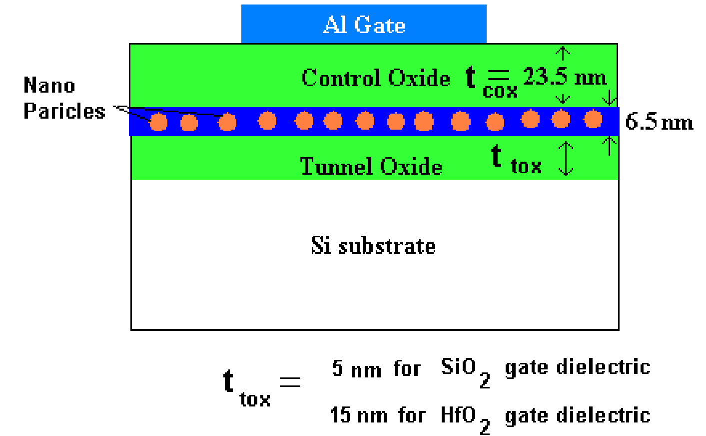
▪Nanocrystal incorporation markedly reduces the onset voltage of F-N tunneling by ~5V-7V Volts.

▪The composite gate dielectric with nc-Ge has a slightly lower value of onset voltage for F-N tunneling compared to the nc-Si embedded one.

Ref: G. Chakraborty, A. Sengupta, F.G. Requejo, C.K. Sarkar, J. Appl. Phys., 109, 064504 (2011).

Modified Floating Gate Approach





Charging of NCs

$$\varphi_1 = \varphi_{10} - \alpha E_{ox}^{1/2} - \beta E_{ox}^{2/3}$$

$$J_{FN} = \left(\frac{q^3 m_{si}}{16\pi^2 m_{ox}\hbar}\right) \cdot \frac{E_{tox}^2}{\varphi_1} \cdot \exp\left\{-\left(\frac{2\sqrt{8m_{ox}q}}{3\hbar}\right)\frac{\varphi_1^{3/2}}{E_{tox}}\right\}$$

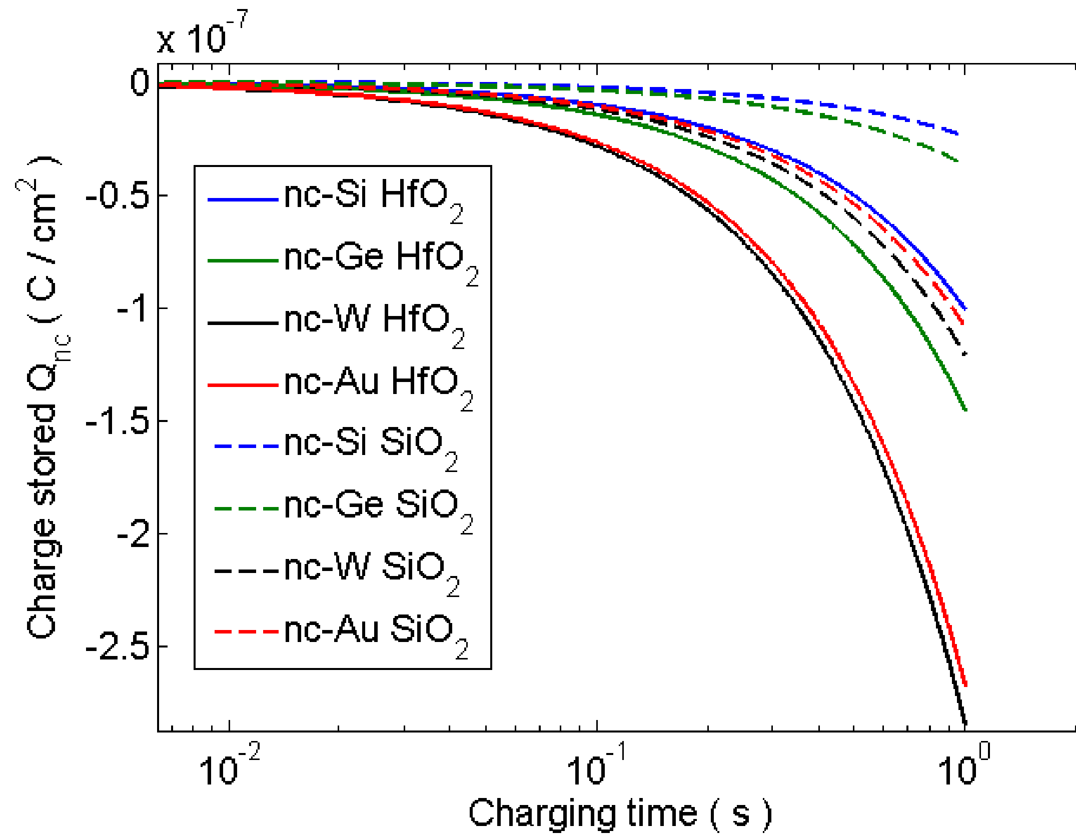
Ref:
A. Sengupta, P. Shah, C.K. Sarkar, F.G. Requejo
Adv. Sci. Lett. (Accepted Article)

Leakage from NC to Si

$$\varphi_2 = \varphi_{20} - \alpha E_{ncox}^{1/2}$$

$$J'_{DT} = \frac{\{2m_{ox}(\varphi_2 - \varepsilon_{nc})\}^{1/2} \alpha q^2 E_{ncox}}{\hbar^2} \exp\left(\frac{2\alpha\sqrt{2m_{ox}(\varphi_2 - \varepsilon_{nc})}}{\hbar} t_{tox}\right)$$

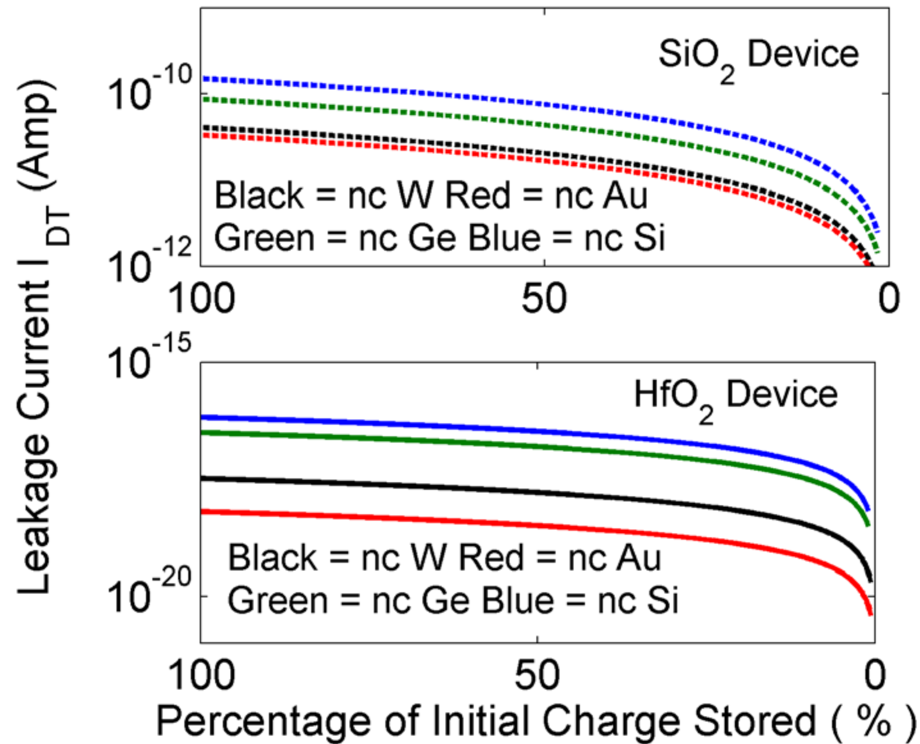
Charge Storage of ncs



- **Metal Nanocrystals store higher amount of charge.**

Ref: A. Sengupta, C.K. Sarkar, F.G. Requejo, Adv. Sci. Lett. (accepted article)

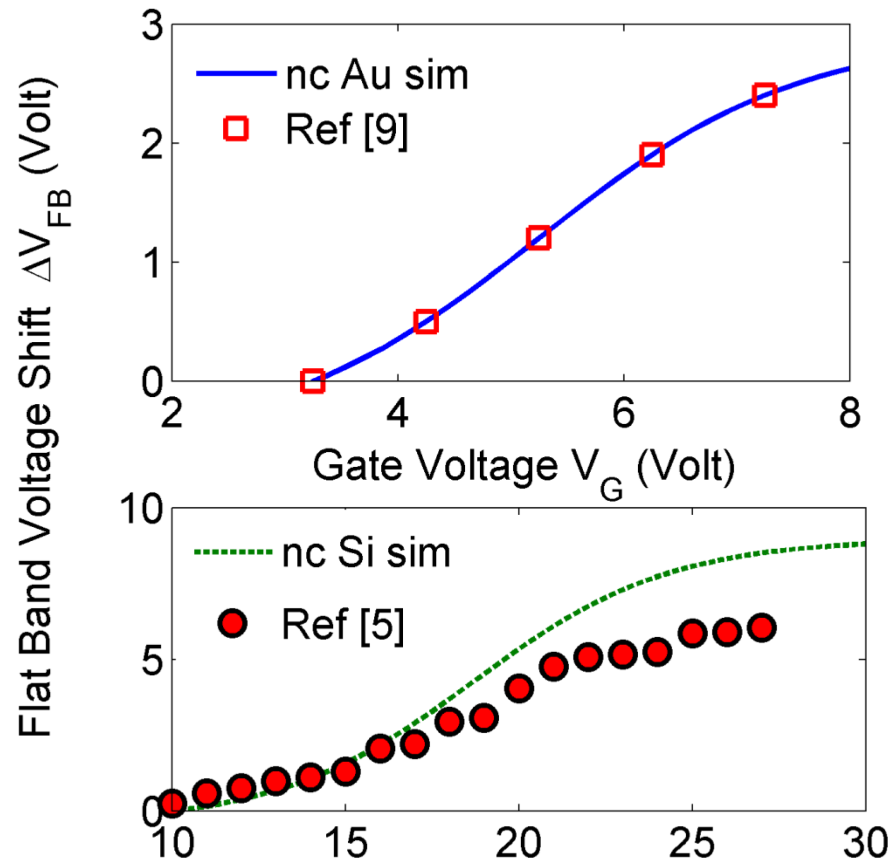
Simulated Leakage currents



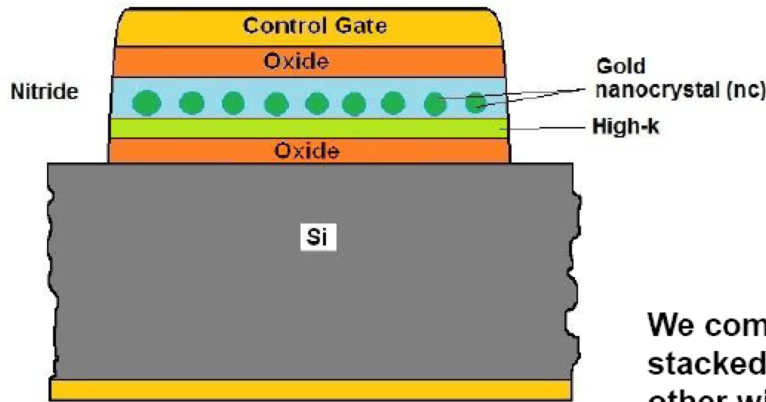
•Metal Nanocrystals offer lesser leakage current compared to Semiconductor ncs.

• Use of High-k dielectrics can further reduce leakage current.

Flat-band Voltage Shift

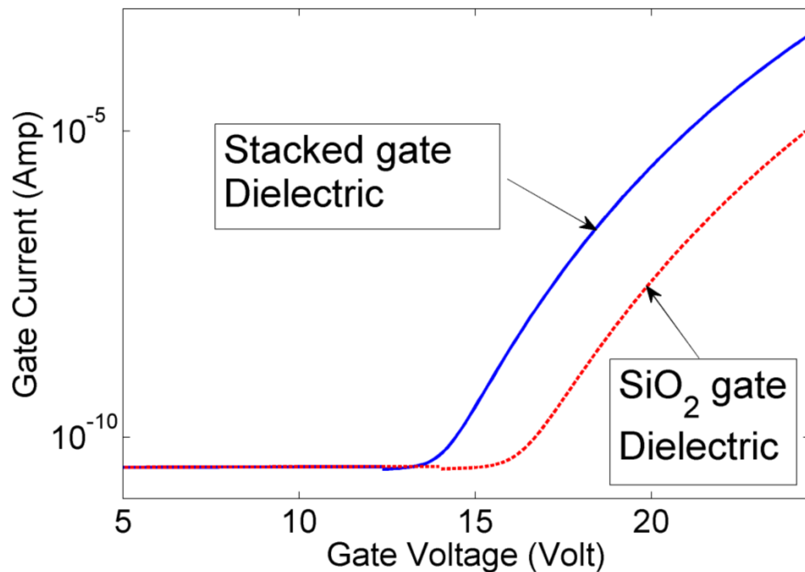


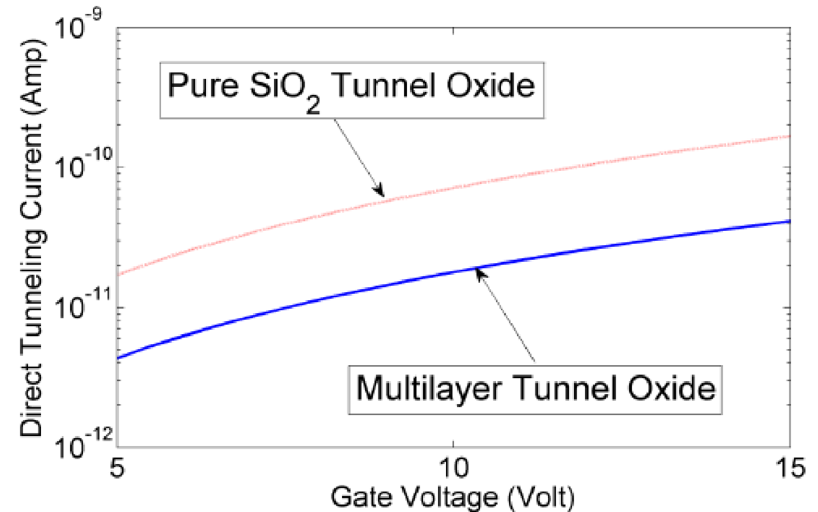
•Flat-band shift simulations show a fair degree of agreement with experimental results.



- Lesser leakage current.
- Same capacitance with thicker tunnel oxide.
- SiO_2 usually used as bottom layer for better lattice matching with Si.

We compare two devices, one with stacked HfO_2-SiO_2 tunnel oxide, the other without stacked tunnel oxide.

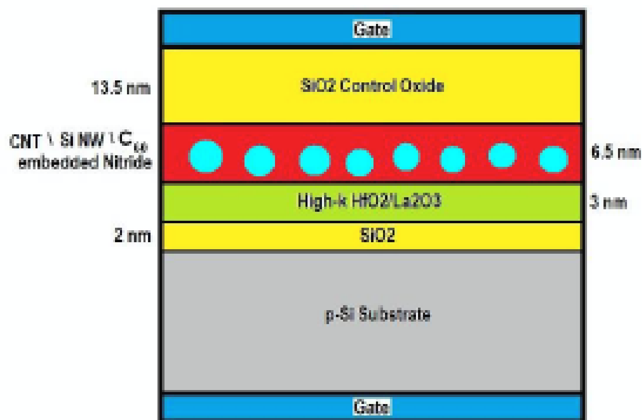


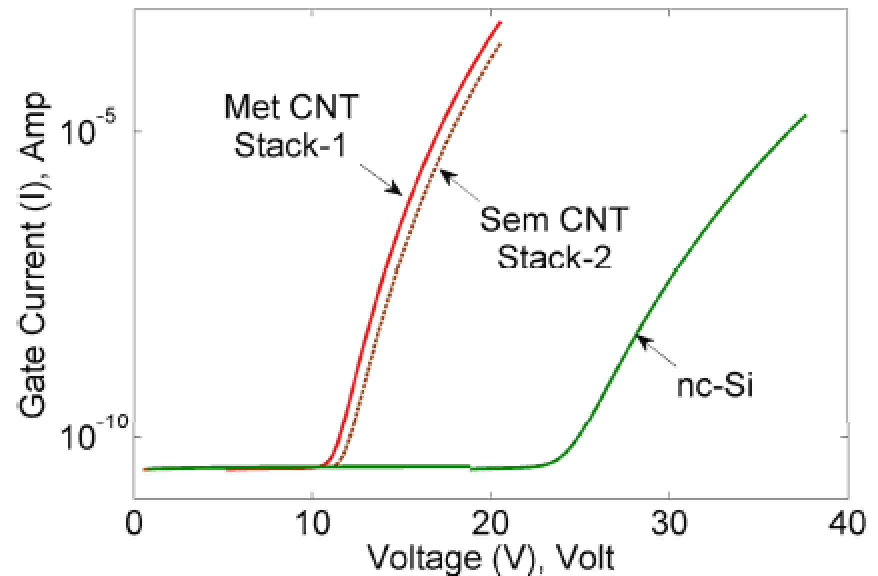


- nc embedded stacked gate devices show better performance than non-stacked structure.

Ref: A. Sengupta, C.K. Sarkar, The 4th IEEE International NanoElectronics Conf. (IEEE INEC), June 21-24, 2011, Taiwan

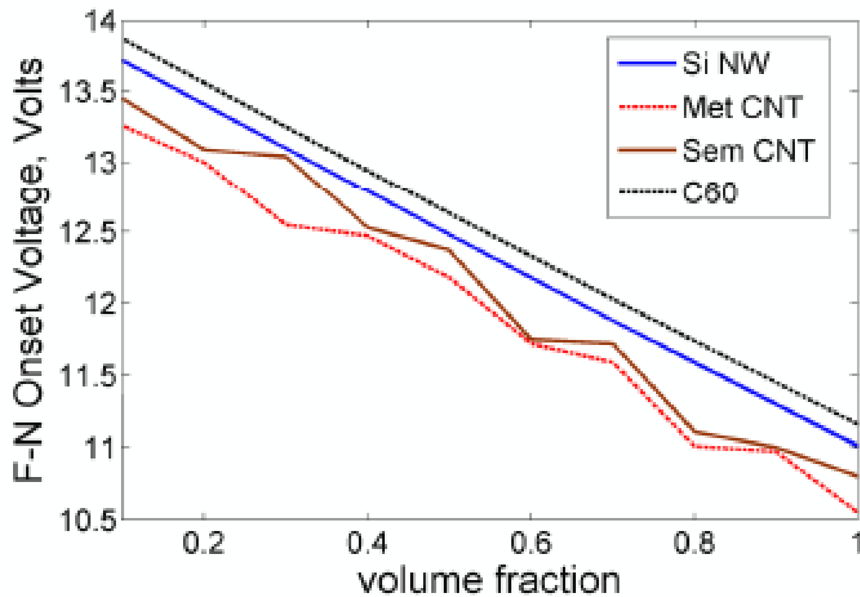
Si Nanowire / CNT / Fullerene Embedded devices





- **CNT / Si NW embedded devices show better performance than nc-Si embedded MOSCAP.**
- **HfO_2 is the better choice in combination with SiO_2 in stacked tunnel oxide.**

Ref: A. Sengupta, C.K. Sarkar, F.G. Requejo, J. Phys. D: Appl. Phys. Vol. 44, No. 36 pp. 405101 (2011).



Study of Write Voltage variation with increasing volume fraction of the embedded nanomaterials.

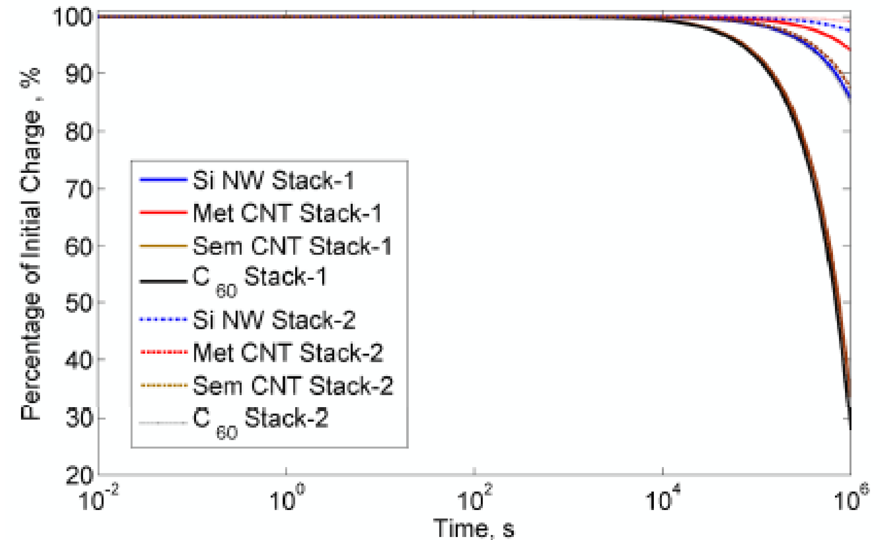


Fig 9: Decay of charge during the waiting time under a gate bias of -0.1 Volts.

Study of charge decay during waiting time for the different structures.

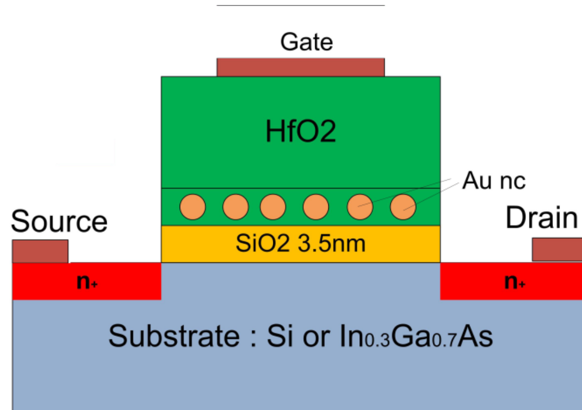
Ref: A. Sengupta, C.K. Sarkar, F.G. Requejo, J. Phys. D: Appl. Phys. Vol. 44, No. 36 pp. 405101 (2011).

Parameter	This Paper			Earlier Work{Ref [10]}
	Met CNT Stack-1	Si NW Stack-1	C60 Stack-1	nc-Si
F-N onset voltage	13.030 Volts	13.208 Volts	13.356 Volts	20.36 Volts
F-N Tunnelling Current (Amps) at 15 Volts	6.205×10^{-7}	4.72×10^{-7} A	3.2×10^{-7} A	1.05×10^{-10} A
Direct Tunnelling Current (Amps) (at 7.5 Volts)	3.179×10^{-11} A	3.184×10^{-11} A	3.237×10^{-11} A	3.320×10^{-11} A

Ref: A. Sengupta, C.K. Sarkar, F.G. Requejo, J. Phys. D: Appl. Phys. Vol. 44, No. 36 pp. 405101 (2011).

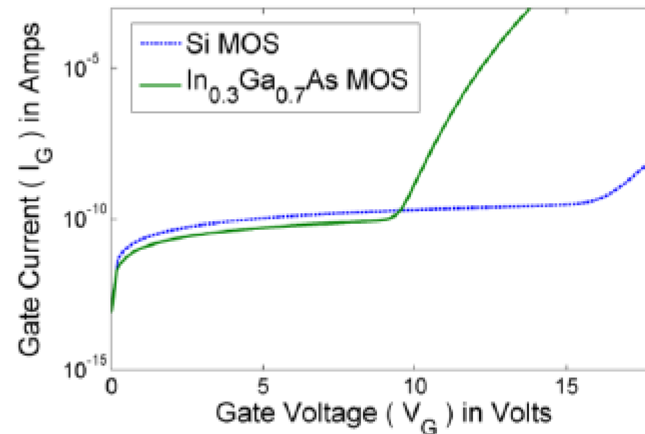
STACK-1 SIMULATION RESULTS					
Embedded nc	Write Voltage (Volt)	F-N Tunnelling Current (Amp) at +15 Volts	Write Time (s) at +14.5 Volts	Retention Time (s)	Erase Time (s) at 15V pulse height
Met CNT	13.030	6.205×10^{-7}	0.150×10^{-4}	2.5×10^{5}	0.149×10^{-4}
Sem CNT	13.169	4.825×10^{-7}	0.193×10^{-4}	2.1×10^{4}	0.176×10^{-4}
Si NW	13.209	4.72×10^{-7}	0.197×10^{-4}	6×10^{4}	0.188×10^{-4}
C-60	13.356	3.2×10^{-7}	0.292×10^{-4}	1.94×10^{4}	0.102×10^{-4}
STACK-2 SIMULATION RESULTS					
Embedded nc	Write Voltage (Volt)	F-N Tunnelling Current (Amp) at +15 Volts	Write Time (s) at +14.5 Volts	Retention Time (s)	Erase Time (s) at 15V pulse height
Met CNT	13.702	2.275×10^{-7}	0.410×10^{-4}	1.15×10^{6}	0.402×10^{-4}
Sem CNT	13.696	2.337×10^{-7}	0.399×10^{-4}	6.35×10^{4}	0.303×10^{-4}
Si NW	13.850	1.607×10^{-7}	0.581×10^{-4}	6.5×10^{5}	0.356×10^{-4}
C-60	13.991	1.352×10^{-7}	0.691×10^{-4}	5.7×10^{4}	0.297×10^{-4}

NC embedded MOSFET NVMs



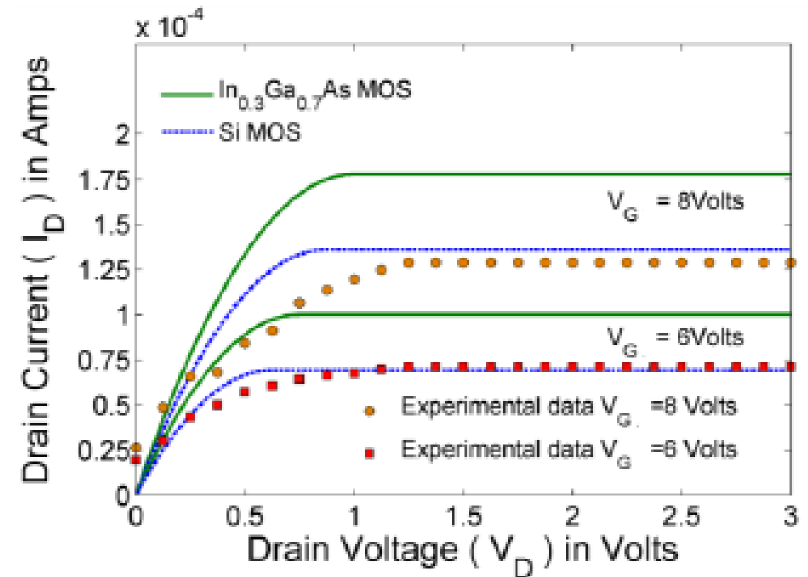
- We also study nc embedded MOSFET NVM devices.
- Au nc was selected for better performance and based on reliability studies.
- We compare Si and $In_{0.3}Ga_{0.7}As$ substrates.

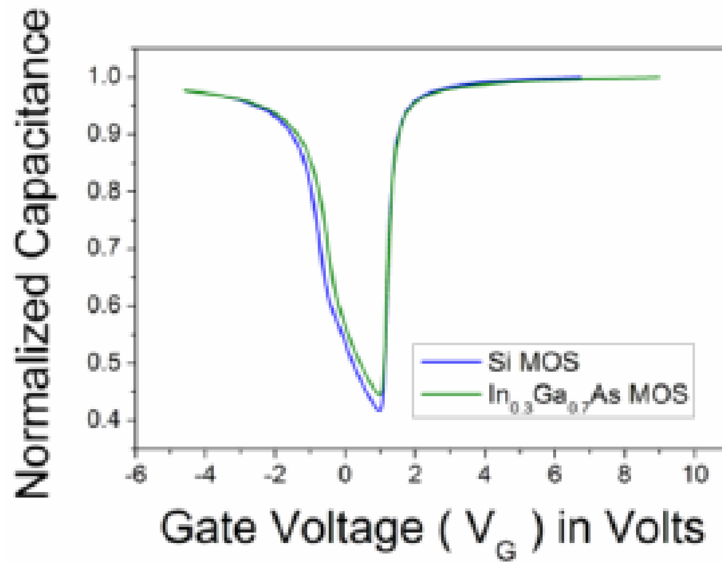
- The compound semiconductor ($In_{0.3}Ga_{0.7}As$) MOSFET NVM shows lesser F-N onset and lesser leakage.
- Write voltages lowered by 3-4 Volts.



Ref: A. Sengupta, C.K. Sarkar , Int. J. Nanotechnol. (2011) {under review}.

- We also simulated the I_D-V_D (output) characteristics.
- Compound semiconductor MOSFET shows higher drain currents.
- The simulated results for Si MOSFET NVM match experimental results of Mikhelashvili et. al. [Appl. Phys. Lett. 98, 212902 (2011)]

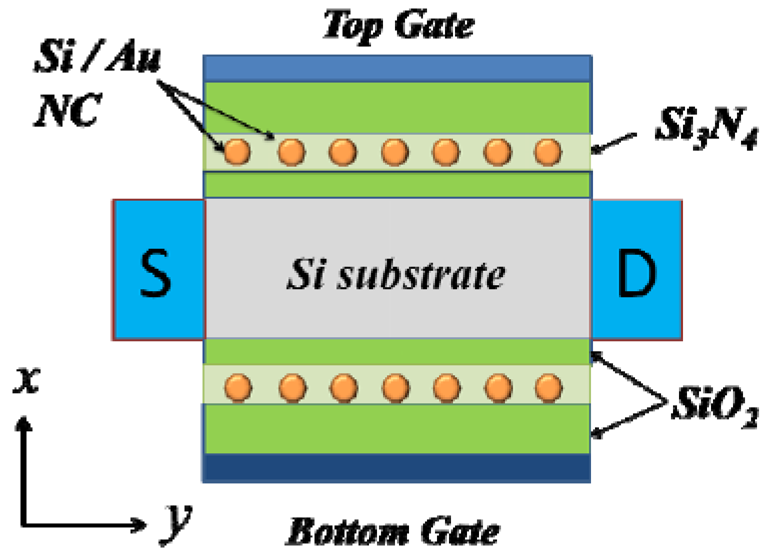




- We also simulated the HFCV characteristics using the Berkeley Devices Simulator.
- Compound semiconductor MOSFET shows slightly higher value of normalized capacitance.

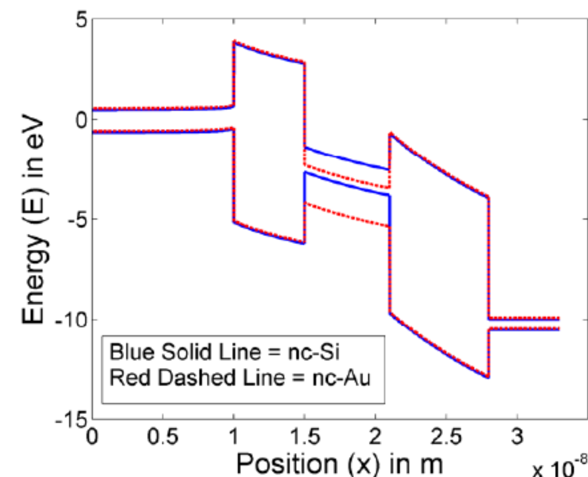
Ref: A. Sengupta, C.K. Sarkar , Int. J. Nanotechnol. (2011) {under review}.

NC embedded DGMOSFET NVMs

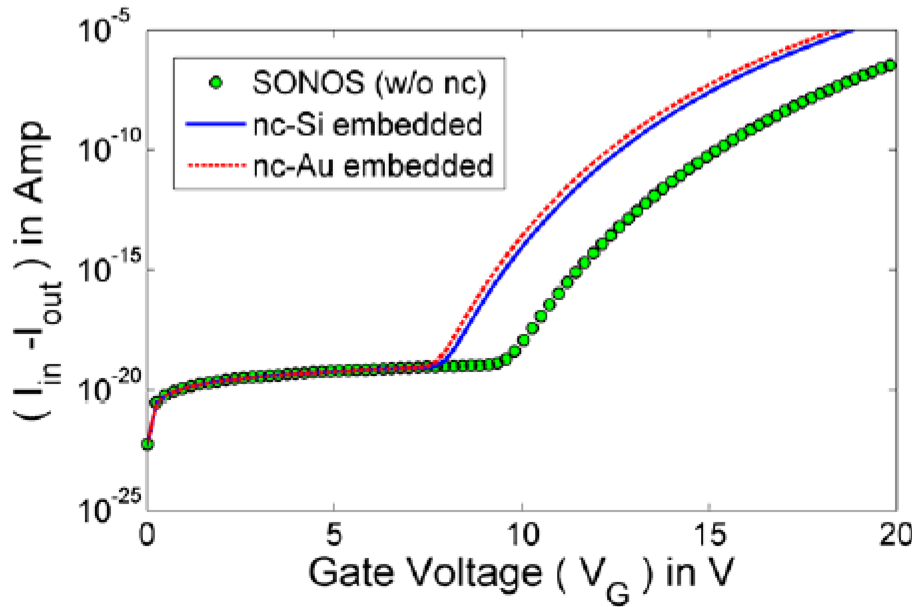


- DGMOSFETs offer better electrostatic control in the channel, than the planar MOS and therefore are becoming more and more popular.
- Most DGMOSFET memories depend on SONOS architecture.
- Nanocrystal embedded dielectric DGMOSFET NVM may be very useful.

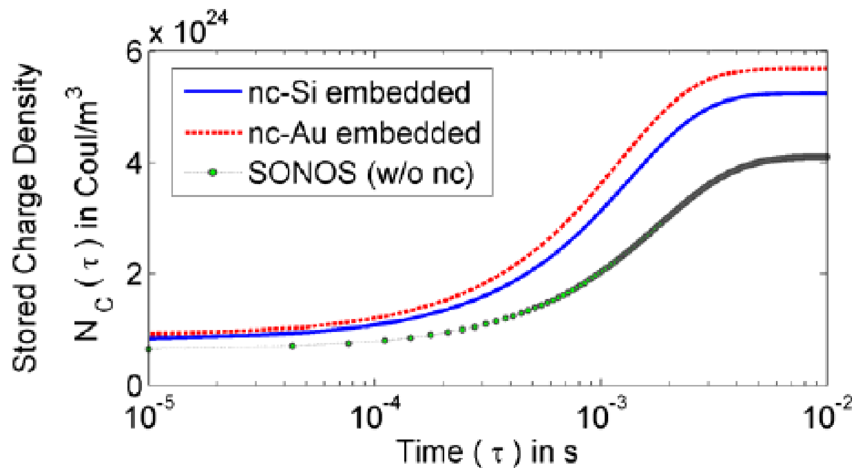
- The energy band diagram of a DGMOSFET NVM under a positive gate bias {simulation results}

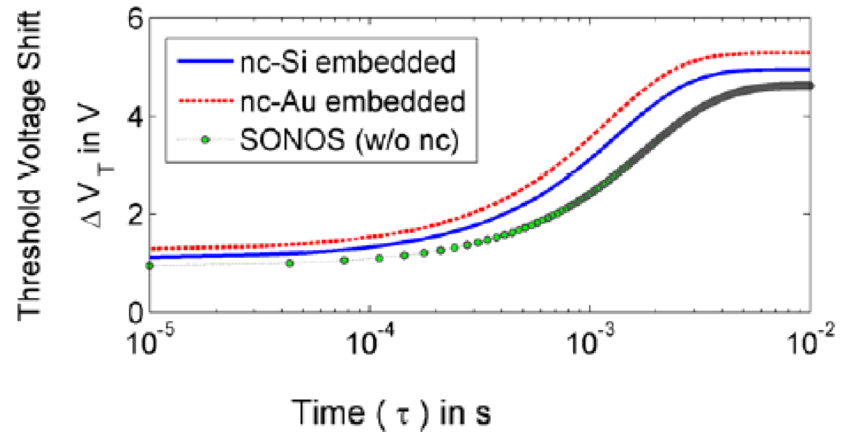


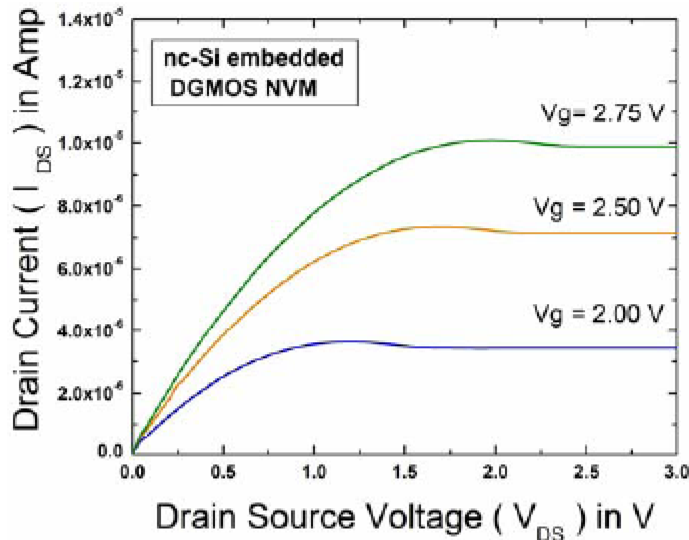
Ref: A. Sengupta, C.K. Sarkar , 'Surface Potential Based Analytical Modeling of Double Gate MOSFET with Si and Au Nano-dots Embedded Gate Dielectric for Non-Volatile Memory Applications' J. Appl. Phys. {Communicated}.

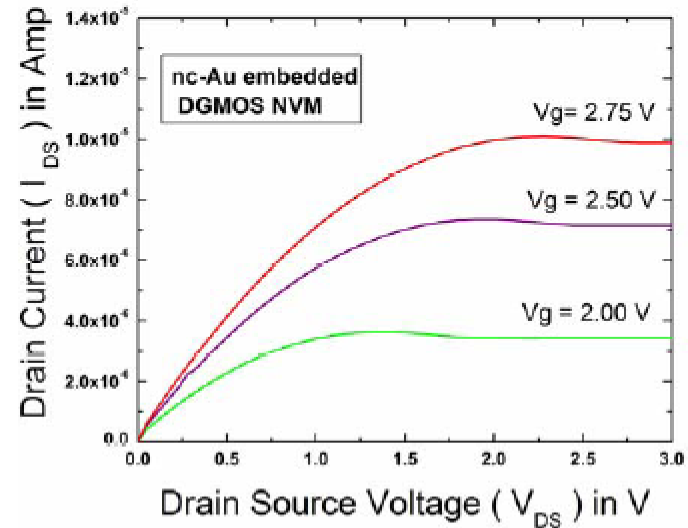


- Nc embedded DGMOSFETs offer better write performance than their SONOS DGMOSFET counterparts, Au nc is the better among the two ncs compared.
- Improvement of ~2V in terms of write voltage.
- Also more charge stored and higher Threshold Voltage (Vth) Shift.





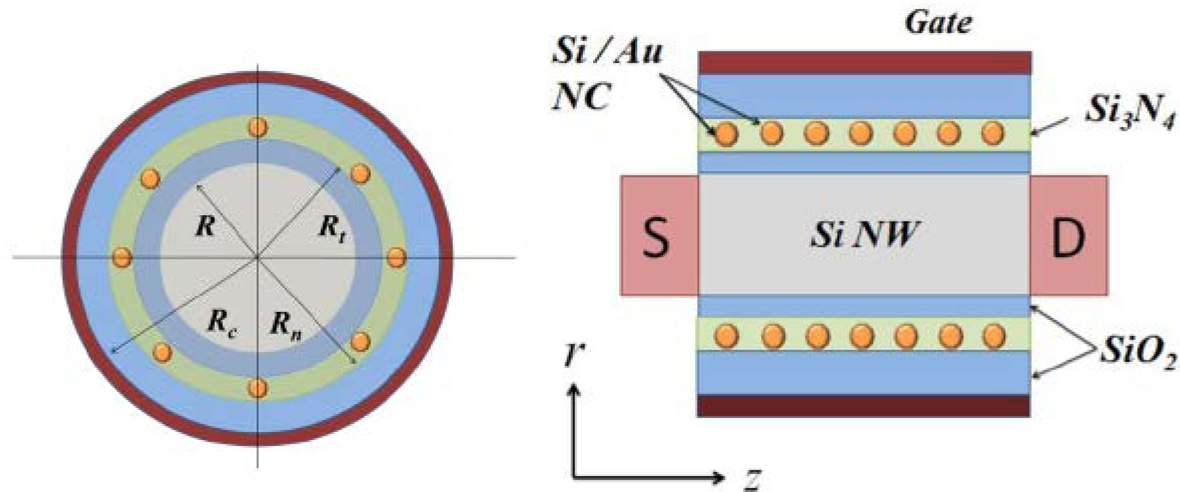




- **Almost similar magnitude of drain currents in the nc-Si and nc-Au embedded devices.**
- **Threshold Voltage of nc-Au embedded DGMOSFET, slightly higher.**
- **Slight tendency of V_{DS} de-clamping due to charging of nanocrsytals.**

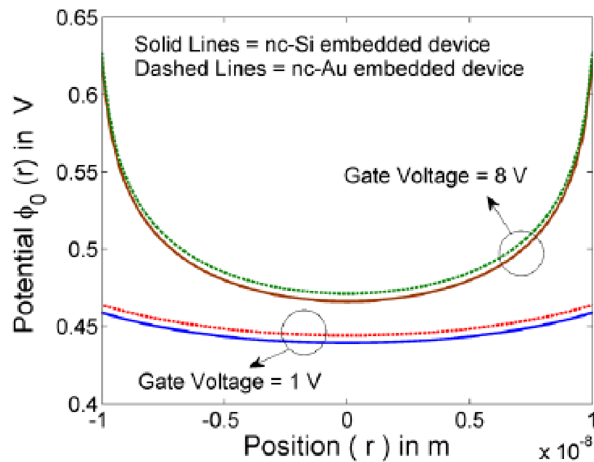
Ref: A. Sengupta, C.K. Sarkar , 'Surface Potential Based Analytical Modeling of Double Gate MOSFET with Si and Au Nano-dots Embedded Gate Dielectric for Non-Volatile Memory Applications' J. Appl. Phys. {Communicated}.

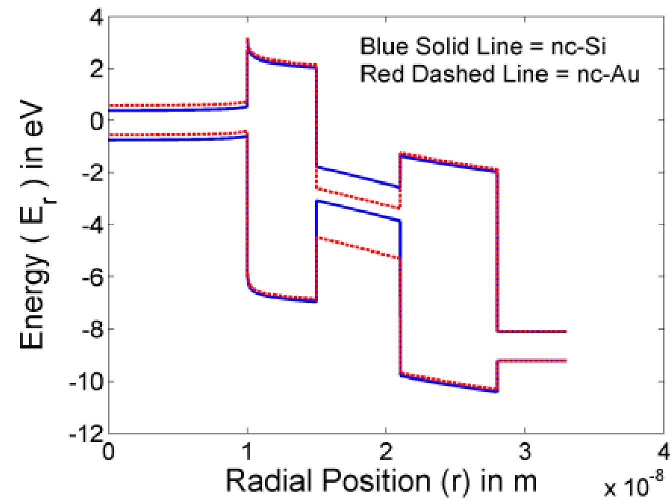
NC embedded GAA MOSFET NVMs



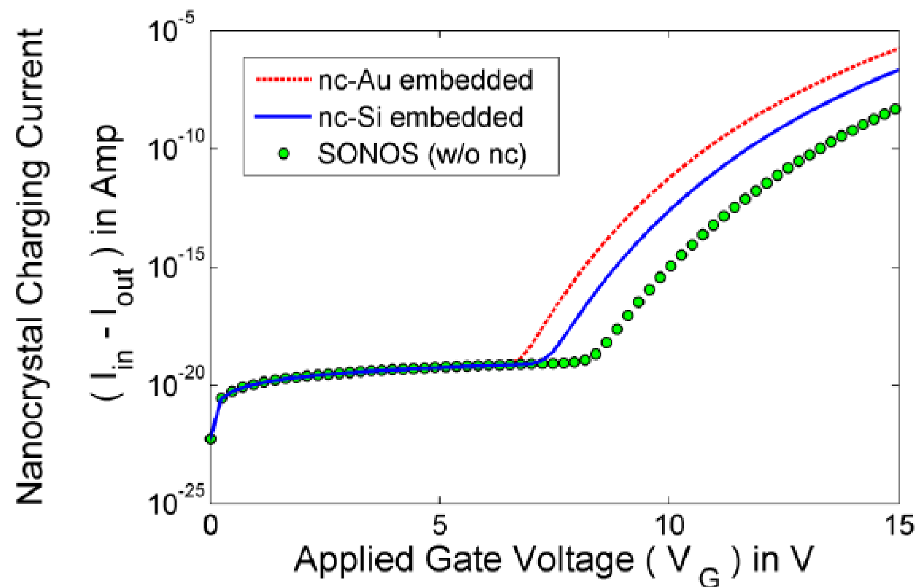
- **We also study GAA (Gate All Around) MOS NVMs.**
- **These structures offer the best electrostatic control over the channel among all the advanced MOSFETs (i.e. better than DGMOS, Fin-FET, Π-Gate, or Ω-gate MOSFETs).**
- **GAA SONOS memories have been reported as well as recent experimental works on nc embedded gate dielectric GAA MOSFET memory.** [Hung. Et. al. Appl. Phys. Lett.98,162108(2011)]

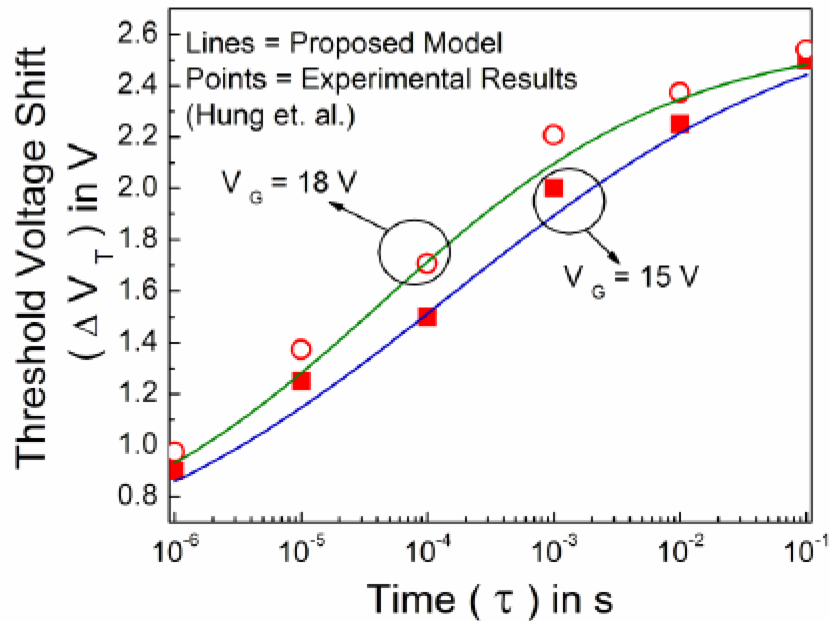
Ref: A. Sengupta, C.K. Sarkar , 'Analytical Modelling of Si and Au Nanocrystal Embedded Multilayer Gate Dielectric Long Channel Silicon Nanowire Surround Gate MOSFET Non Volatile Memory Devices' *J. Phys. D: Appl. Phys. {Communicated}.*

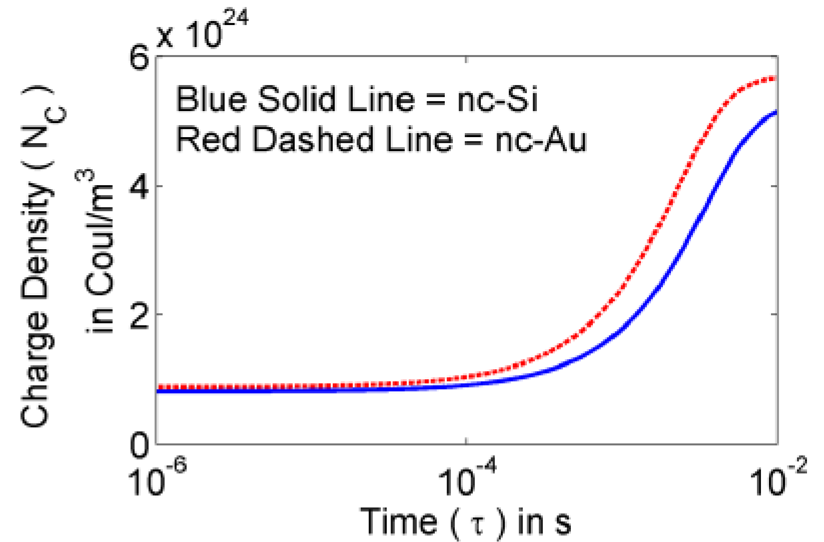


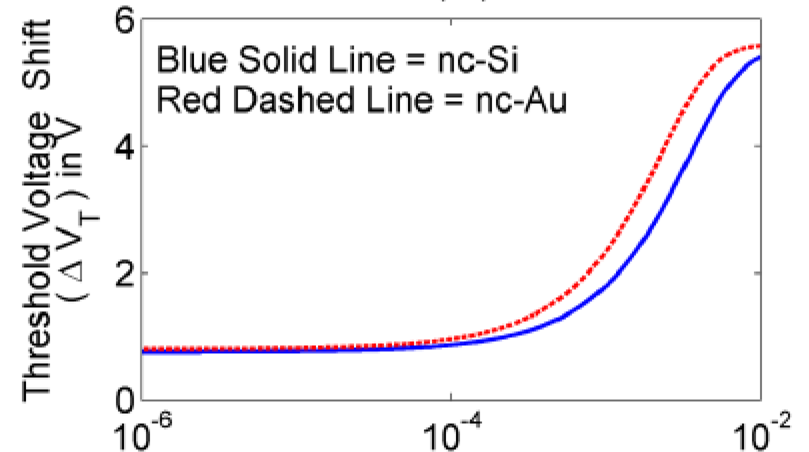


- **We simulated the surface potentials, energy band diagrams, and the write voltages of Si and Au nc embedded gate dielectric GAA MOSFET NVMs.**

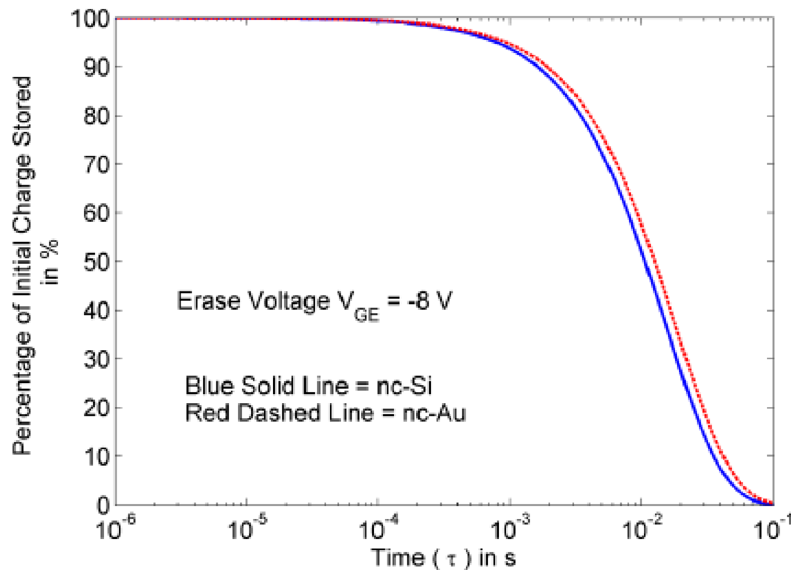




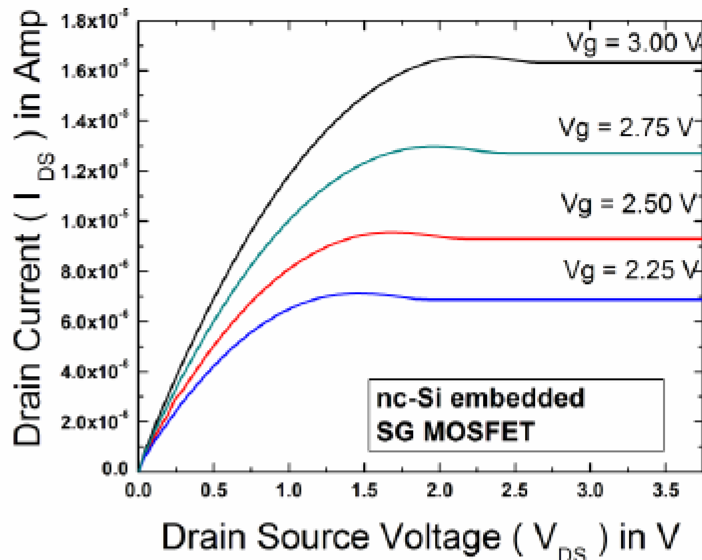


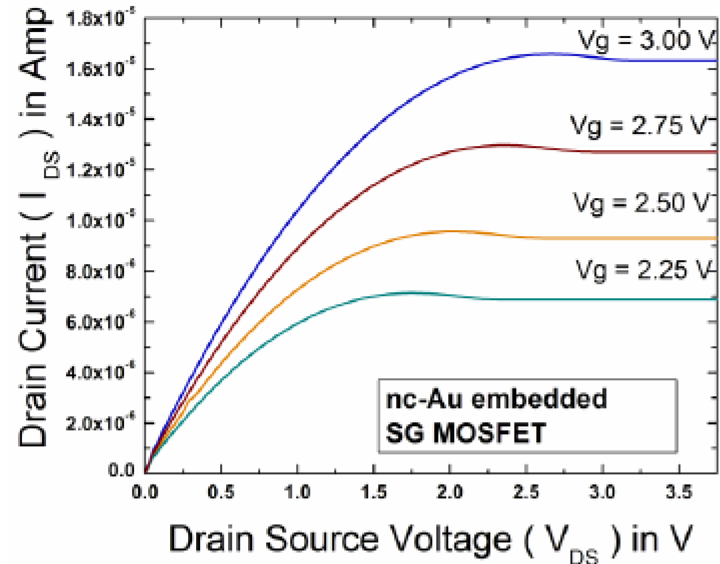


- **Also more charge stored and higher Threshold Voltage (Vth) Shift with nc-Au embedded GAA MOSFET memory device.**
- **The simulations tally well with experimental results by Hung et. al.**



- Nc-Au is also the better performer in terms of charge retention.
- Therefore we may propose the use of nc-Au in nc embedded gate oxide GAA MOSFET NVM.





Conclusions

- MOS NVM devices are extensively used in flash memory based gadgets and computers.
- Floating Gate MOS memory elements mostly employed in flash memory devices.
- Conventional Floating Gate MOS NVMs suffer from leakage, also write voltages need to be lowered.
- Nanocrystals embedded Floating Gate MOS devices apply nanotechnology to improve device performance.
- Nc embedded MOS NVMs show lesser leakage current and lower write voltages compared to conventional MOS NVMs.
- Metal ncs and High-k dielectrics can improve the situation further.
- Nc embedded MOS NVMs may be the memory device of choice in near future.

Thank You

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